

TEA1795T

GreenChip synchronous rectifier controller

Rev. 1 — 4 November 2010

Product data sheet

1. General description

The TEA1795T is a member of the new generation of Synchronous Rectifier (SR) controller ICs for switched mode power supplies. Its high level of integration enables the design of a cost-effective power supply with a minimum number of external components.

The TEA1795T is a dedicated controller IC for synchronous rectification on the secondary side of resonant converters. It has two driver stages for driving the SR MOSFETs, which are rectifying the outputs of the central tap secondary transformer windings.

The two gate driver stages have their own sensing inputs and operate independently of each other.

The TEA1795T is fabricated in a Silicon On Insulator (SOI) process.

2. Features and benefits

2.1 Distinctive features

- Accurate synchronous rectification functionality
- Wide supply voltage range (8.5 V to 38 V)
- Separate sense inputs for sensing the drain and source voltage of each SR MOSFET
- High level of integration, resulting in a minimum external component count
- High driver output voltage of 10 V to drive all MOSFET brands to the lowest R_{DSon}

2.2 Green features

- Low current consumption
- High system efficiency from no load to full load

2.3 Protection features

- UnderVoltage Protection (UVP)

3. Applications

The TEA1795T is intended for resonant power supplies. In such applications, it can drive two external synchronous rectifier MOSFETs which replace diodes for the rectification of the voltages on the two secondary windings of the transformer. It can be used in applications such as:

- Adapters
- ATX power supplies



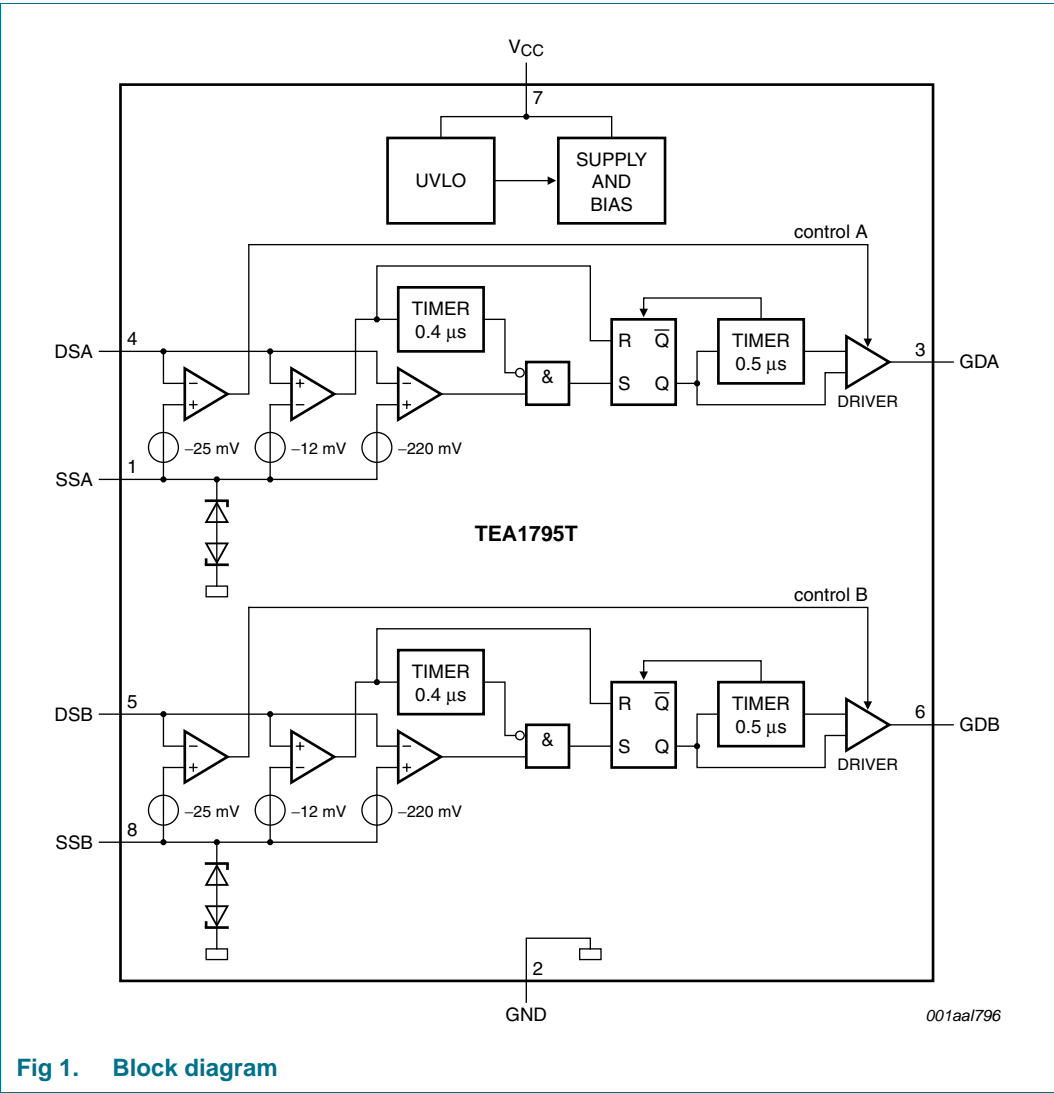
- Server power supplies
- LCD television
- Plasma television

4. Ordering information

Table 1. Ordering information

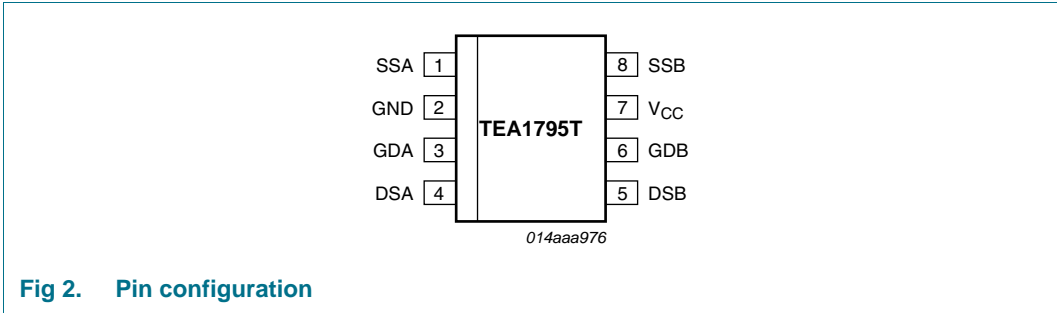
Type number	Package		Version
	Name	Description	
TEA1795T/N1	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

5. Block diagram



6. Pinning information

6.1 Pinning



6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
SSA	1	source sense input MOSFET A
GND	2	ground
GDA	3	gate driver output MOSFET A
DSA	4	drain sense input for synchronous timing MOSFET A
DSB	5	drain sense input for synchronous timing MOSFET B
GDB	6	gate driver output MOSFET B
V _{CC}	7	supply voltage
SSB	8	source sense input MOSFET B

7. Functional description

7.1 Introduction

The TEA1795T is a controller for synchronous rectification to be used in resonant applications. It can drive two synchronous rectifier MOSFETs on the secondary side of the central tap transformer winding. A typical configuration is shown in [Figure 3](#).

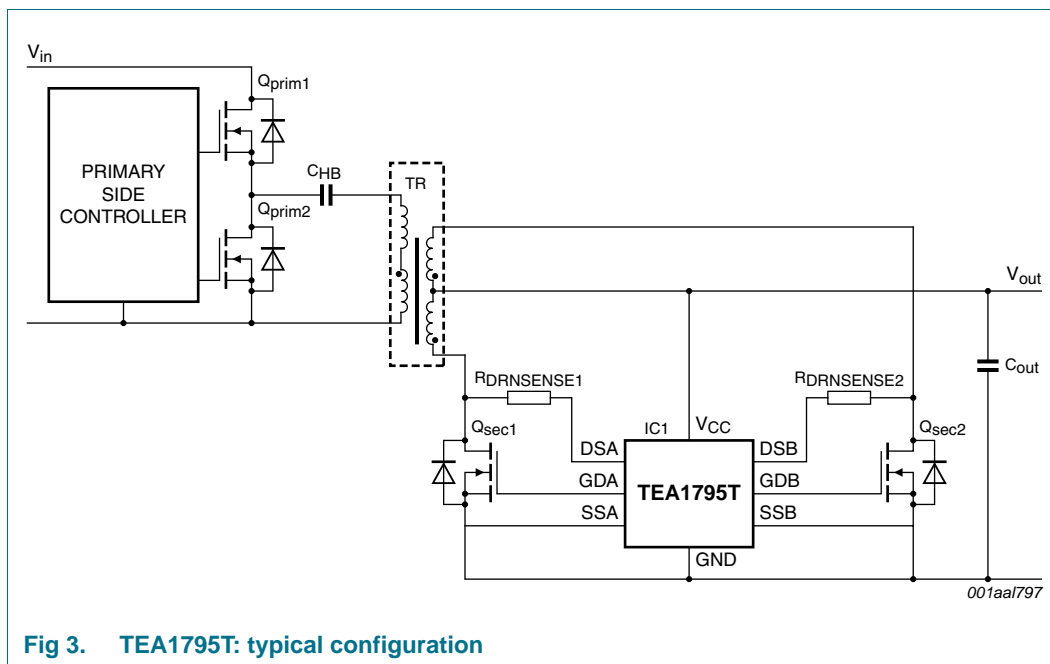


Fig 3. TEA1795T: typical configuration

7.2 Start-up and UnderVoltage LockOut (UVLO)

The IC leaves the UVLO state and activates the synchronous rectifier circuitry when the voltage on the V_{CC} pin is above $V_{startup}$ (8.5 V typical). When the voltage drops below 8.0 V (typical), the UVLO state is reentered and the SR MOSFET gate driver outputs are actively kept low.

7.3 Supply management

All (internal) reference voltages are derived from a temperature compensated, on-chip band gap circuit.

7.4 Synchronous rectification (DSA, SSA, DSB and SSB pins)

The voltages present between the drain and source terminals of the SR MOSFETs are used to derive the timing for the gate drive signal. The IC senses the voltage difference between the drain sense (pins DSA and DSB) and the source sense (pins SSA and SSB) connections. When this voltage difference is lower than $V_{act(drv)}$ (−220 mV typical), the corresponding gate driver output voltage is driven high and the external SR MOSFET is switched on.

When the external SR MOSFET is switched on, the input signals on the drain sense pins and source sense pins are ignored during the minimum synchronous rectification active time ($t_{act(sr)(min)}$, 520 ns typical). This minimizes false switch-off due to the sensing of high frequency ringing signals at the start of the conduction phase.

Once this minimum synchronous rectification active time has ended, the IC monitors the difference between the drain sense inputs and the source sense inputs. When the difference is higher than $V_{reg(drv)}$ (−25 mV typical), the gate driver output voltage is regulated to maintain this −25 mV difference between the drain sense pins and the source sense pins. As a result, the SR MOSFET can be switched off quickly when the current through the external SR MOSFET reaches zero.

The zero current is detected by sensing a $V_{\text{deact}(\text{drv})}$ (–12 mV typical) difference between the drain sense pins and the source sense pins (see [Figure 4](#)). A synchronous rectification off-timer ($t_{\text{off}(\text{sr})}(\text{min})$, 400 ns typical) is started and the next switching cycle can only be started when the synchronous rectification off-timer has finished.

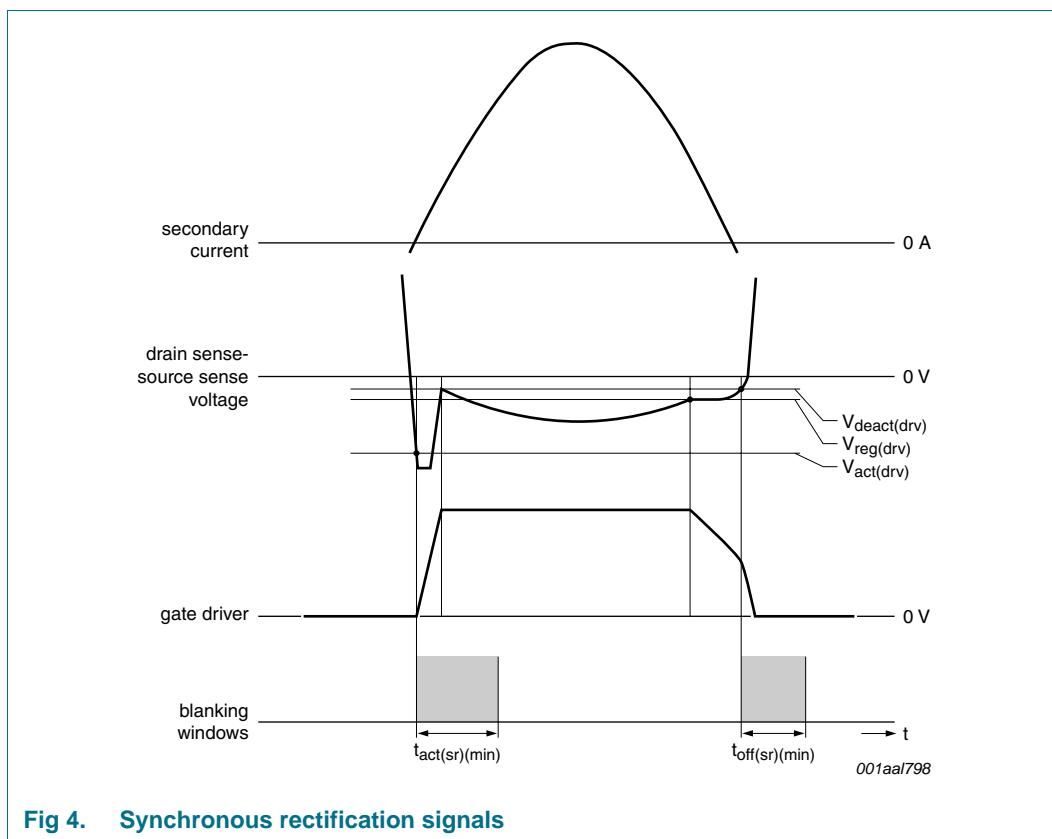


Fig 4. Synchronous rectification signals

7.5 Gate driver (GDA and GDB pins)

The gate driver circuit to the gate of the external SR MOSFET has a source capability of typically 400 mA and a sink capability of typically 2.7 A. This allows fast turn-on and turn-off of the external SR MOSFET for efficient operation. The source stage is coupled to the timer (see [Figure 1](#)). When the timer has finished, the source capability is reduced to a small current (4 mA typical) capable of keeping the driver output voltage at its level.

The output voltage of the driver is limited to 10 V (typical). This high output voltage drives all MOSFET brands to the minimum on-state resistance.

During start-up conditions ($V_{\text{CC}} < V_{\text{startup}}$) and UVLO the driver output voltage is actively pulled low.

7.6 Source sense (SSA and SSB pins)

The IC is equipped with additional source sense pins (SSA and SSB). These pins are used for the measurement of the drain-to-source voltage of the external SR MOSFET. This drain-to-source voltage determines the timing of the gate driver. The source sense input should be connected as close as possible to the source pin of the external SR MOSFET to minimize timing errors, caused by voltage difference on PCB tracks, due to parasitic inductance in combination with large di/dt values.

8. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are measured with respect to ground (pin 2); positive currents flow into the chip. Voltage ratings are valid provided other ratings are not violated; current ratings are valid provided the other ratings are not violated.

Symbol	Parameter	Conditions	Min	Max	Unit
Voltages					
V_{CC}	supply voltage	continuous	-0.4	+38	V
$V_{sense(D)A}$	drain sense voltage A	continuous	-	120	V
$V_{sense(D)B}$	drain sense voltage B	continuous	-	120	V
Currents					
$I_{drv(G)A}$	gate driver current A	$\delta < 10\%$	-0.8	+3.0	A
$I_{drv(G)B}$	gate driver current B	$\delta < 10\%$	-0.8	+3.0	A
$I_{I(DSA)}$	input current on pin DSA		-3	-	mA
$I_{I(DSB)}$	input current on pin DSB		-3	-	mA
$I_{I(SSA)}$	input current on pin SSA		-1	+1	mA
$I_{I(SSB)}$	input current on pin SSB		-1	+1	mA
General					
P_{tot}	total power dissipation	$T_{amb} < 80\text{ }^{\circ}\text{C}$	-	0.45	W
T_{stg}	storage temperature		-55	+150	$^{\circ}\text{C}$
T_j	junction temperature		-40	+150	$^{\circ}\text{C}$
ElectroStatic Discharge voltage (ESD)					
V_{ESD}	electrostatic discharge voltage	class 2			
		human body model [1]	-	2000	V
		machine model [2]	-	200	V
		charged device model	-	500	V

[1] Equivalent to discharging a 100 pF capacitor through a 1.5 k Ω series resistor.

[2] Equivalent to discharging a 200 pF capacitor through a 0.75 μH coil and a 10 Ω resistor.

9. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC test board	150	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	JEDEC test board	100	K/W

10. Characteristics

Table 5. Characteristics

$T_{amb} = 25\text{ }^{\circ}\text{C}$; $V_{CC} = 20\text{ V}$; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply voltage management (pin V _{CC})						
V _{startup}	start-up voltage		8.2	8.5	8.8	V
V _{hys}	hysteresis voltage		[1]	0.5	-	V
I _{CC(oper)}	operating supply current	V _{CC} = 8 V (V _{CC} < V _{startup})	-	0.35	-	mA
		f _{sw} = 200 kHz; no load on pins GDA and GDB	-	1.85	-	mA
Synchronous rectification sense input (pins DSA/SSA and pins DSB/SSB)						
V _{act(drv)}	driver activation voltage	V _{sense(S)A} = 0 V; V _{sense(S)B} = 0 V	−260	−220	−180	mV
V _{reg(drv)}	driver regulation voltage	V _{sense(S)A} = 0 V; V _{sense(S)B} = 0 V	−33	−25	−17	mV
V _{deact(drv)}	driver deactivation voltage	V _{sense(S)A} = 0 V; V _{sense(S)B} = 0 V	[2]	−12	-	mV
V _{I(cm)}	common-mode input voltage	pins SSA and SSB	−0.7	-	+0.7	V
t _{d(act)(drv)}	driver activation delay time	V _{sense(S)A} = 0 V; V _{sense(S)B} = 0 V; V _{sense(D)A} = falling from +0.5 V to −0.5 V; V _{sense(D)B} = falling from +0.5 V to −0.5 V	-	100	-	ns
t _{d(deact)(drv)}	driver deactivation delay time	V _{sense(S)A} = 0 V; V _{sense(S)B} = 0 V; V _{sense(D)A} = rising from −0.35 V to +0.5 V; V _{sense(D)B} = rising from −0.35 V to +0.5 V	-	35	-	ns
t _{act(sr)(min)}	minimum synchronous rectification active time		415	520	625	ns
t _{off(sr)(min)}	minimum synchronous rectification off-time		310	400	490	ns
Gate driver (pins GDA/GDB)						
I _{source}	source current	V _{CC} = 15 V; pins GDA/GDB = 2 V; during minimum synchronous rectification active time	−0.46	−0.4	−0.34	A
		V _{CC} = 15 V; pins GDA/GDB = 5 V; minimum synchronous rectification active time has ended	-	−4	-	mA
I _{sink}	sink current	V _{CC} = 15 V				
		pins GDA/GDB = 2 V	1	1.4	-	A
		pins GDA/GDB = 9.5 V	2.2	2.7	-	A
V _{o(max)}	maximum output voltage	V _{CC} = 15 V	-	10	12	V
Switching						
f _{sw(max)}	maximum switching frequency		500	-	-	kHz

[1] The V_{CC} stop voltage is $V_{startup} - V_{hys}$.

[2] The $V_{deact(drv)}$ level is always above the $V_{reg(drv)}$ level.

11. Application information

A switched mode power supply with the TEA1795T consists of a primary side half bridge, a transformer, a resonant capacitor and an output stage. In the output stage SR MOSFETs are used to obtain low conduction loss rectification. These SR MOSFETs are controlled by the TEA1795T.

The timing for the synchronous rectifier switch is derived from the voltage difference between the corresponding drain sense and source sense pins. The resistor in the drain sense connection is needed to protect the TEA1795T against excessive voltages. These resistors should typically be 1 k Ω . Higher values might impair correct timing, lower values may not provide sufficient protection.

Special attention should be paid to the connection of the drain sense and source sense pins. The voltages measured on these pins are used for the timing of the gate driver output. Wrong measurement results in wrong timing. The connections to these pins should not interfere with the power wiring. The power wiring conducts currents with high di/dt values. This can easily cause measurement errors resulting from induced voltages due to parasitic inductances. The separate source sense pins make it possible to sense the source voltage of the external MOSFETs directly, without having to use the current carrying power ground tracks for this.

11.1 Application diagram resonant application

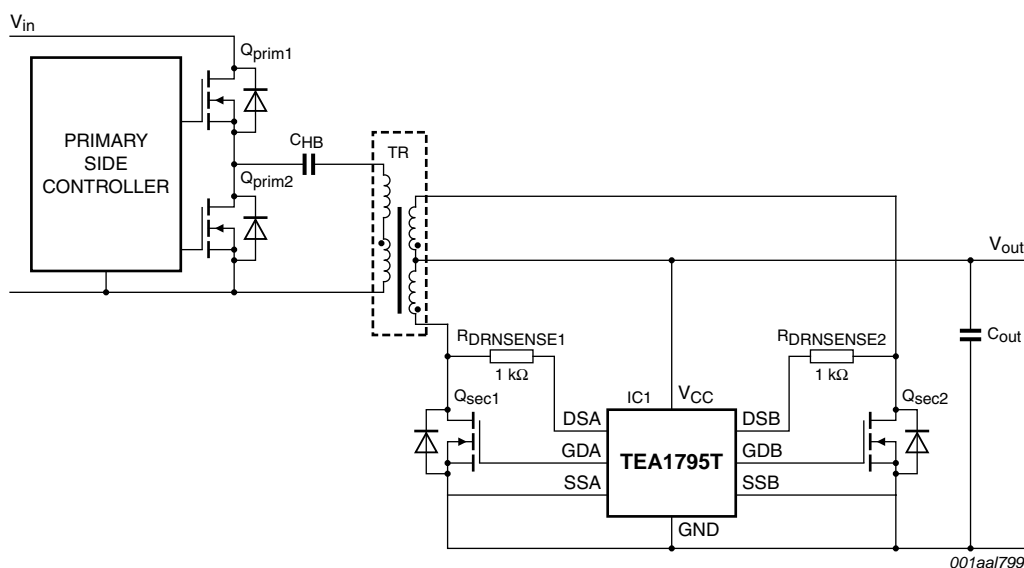
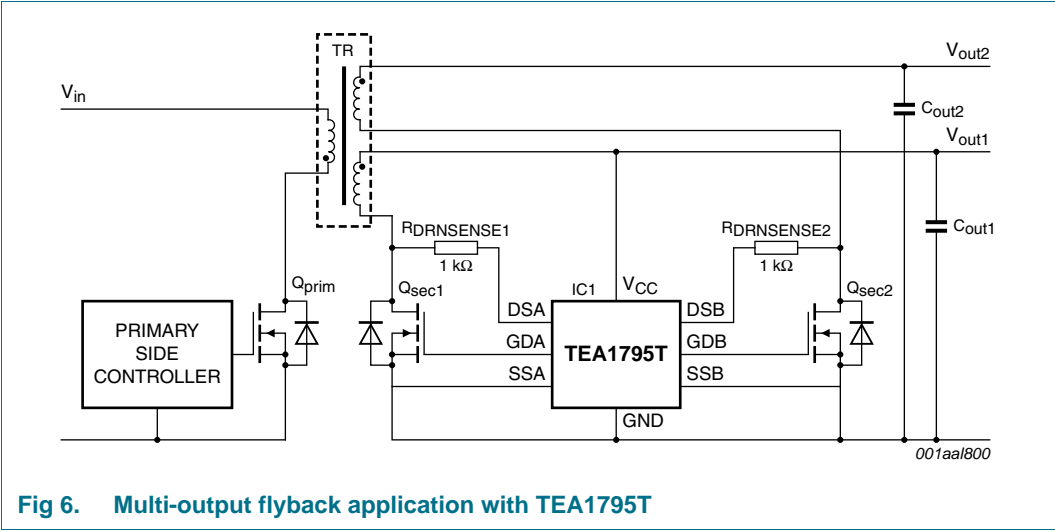


Fig 5. Typical resonant application with TEA1795T

11.2 Application diagram multi-output flyback application



12. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1

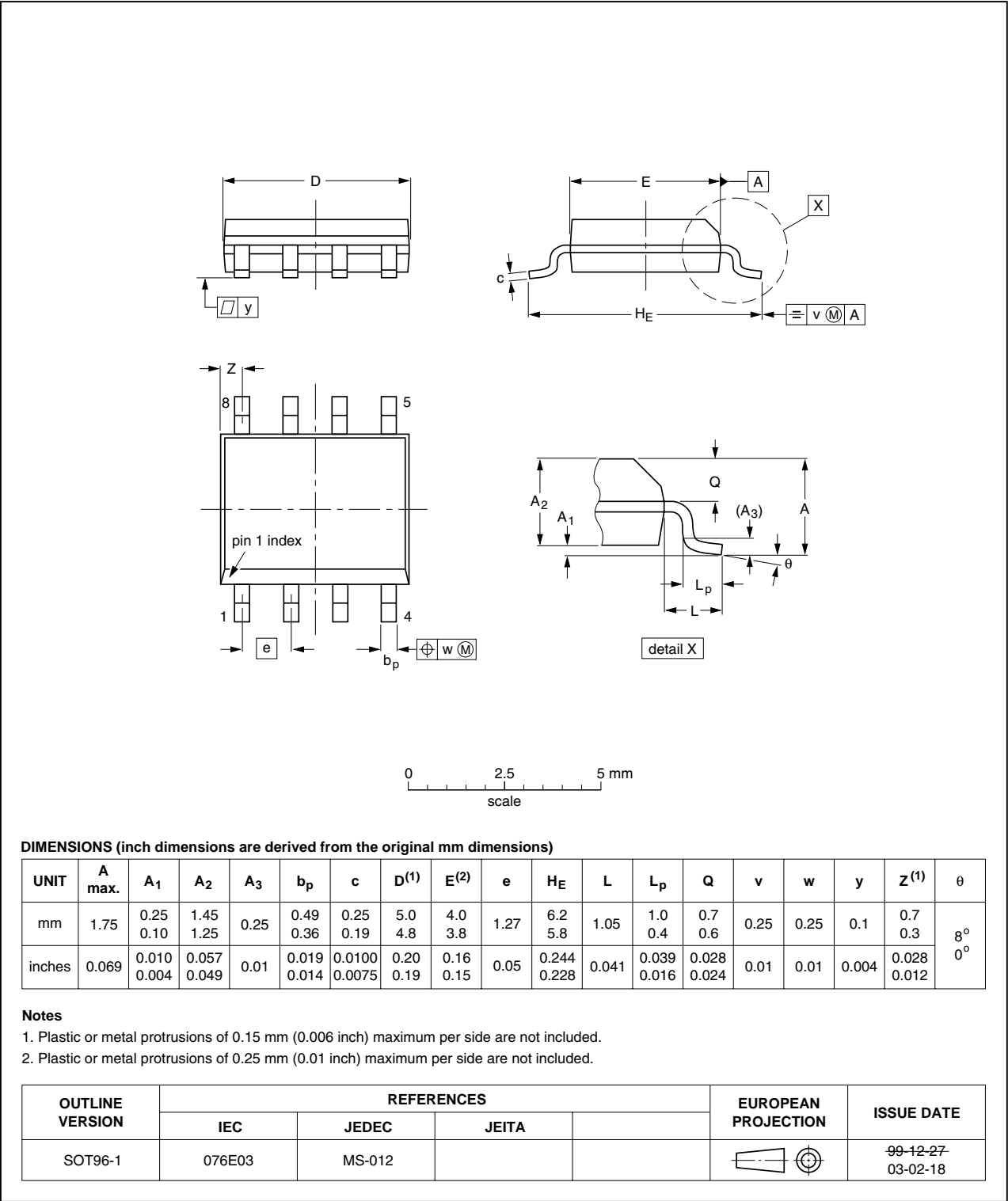


Fig 7. Package outline SOT096-1 (SO8)

13. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TEA1795T v.1	20101104	Product data sheet	-	-

14. Legal information

14.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

14.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

14.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or

malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's

own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

14.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

GreenChip — is a trademark of NXP B.V.

15. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

16. Contents

1	General description	1
2	Features and benefits	1
2.1	Distinctive features	1
2.2	Green features	1
2.3	Protection features	1
3	Applications	1
4	Ordering information	2
5	Block diagram	2
6	Pinning information	3
6.1	Pinning	3
6.2	Pin description	3
7	Functional description	3
7.1	Introduction	3
7.2	Start-up and UnderVoltage LockOut (UVLO) . .	4
7.3	Supply management	4
7.4	Synchronous rectification (DSA, SSA, DSB and SSB pins)	4
7.5	Gate driver (GDA and GDB pins)	5
7.6	Source sense (SSA and SSB pins)	5
8	Limiting values	6
9	Thermal characteristics	6
10	Characteristics	7
11	Application information	8
11.1	Application diagram resonant application	8
11.2	Application diagram multi-output flyback application	9
12	Package outline	10
13	Revision history	11
14	Legal information	12
14.1	Data sheet status	12
14.2	Definitions	12
14.3	Disclaimers	12
14.4	Trademarks	13
15	Contact information	13
16	Contents	14

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2010.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 4 November 2010

Document identifier: TEA1795T