

**TENTATIVE**

All information in this technical data sheet is tentative  
and subject to change without notice.

**15.0"XGA**

**TECHNICAL SPECIFICATION**

**AA150XC01**

**mitsubishi / adi**

Date: Dec.14,'00

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## 1. OVERVIEW

AA150XC01 is 15.0 " color TFT-LCD (Thin Film Transistor Liquid Crystal Display) modules composed of LCD panel, driver ICs, control circuit, and backlight unit.

By applying 8bit digital data, 1 024 × 768, 16.7M-color images are displayed on the 15.0" diagonal screen. Input power voltages are 5.0V for LCD driving.

The type of data and control signals are digital, and 2 pixel data are transmitted per Typ. 32.5 MHz clock cycle.

General specifications are summarized in the following table:

ITEM	SPECIFICATION
Display Area (mm)	304.1(H) × 228.1 (V) (15.0-inch diagonal)
Number of Dots	1024 × 3 (H) × 768 (V)
Pixel Pitch (mm)	0.297 (H) × 0.297 (V)
Color Pixel Arrangement	RGB vertical stripe
Display Mode	normally white TN
Number of Color	16.7M(8 bits/color)
Brightness	300 cd/m <sup>2</sup> (Typ.)
Wide Viewing Angle Technology	Optical Compensation Film
Viewing Angle	-75~75°(H) -60~50°( V)
Surface Treatment	Anti-glare and hard-coating 3H
Electrical Interface	CMOS(VI=3~5V, 2pixel / clock)
Optimum Viewing Angle(Contrast ratio)	6 o'clock
Module Size (mm)	326.0 (W) × 255.0 (H) × 15.5 (D)
Module Mass (g)	1350
Backlight Unit	CCFL, 4-tubes, edge-light, replaceable

Characteristic value without any note is typical value.

The LCD product described in this specification is designed and manufactured for the standard use in OA equipment and consumer products, such as computers, communication equipment, industrial robots, AV equipment and so on.

Do not use the LCD product for the equipment that require the extreme high level of reliability, such as aerospace applications, submarine cables, nuclear power control systems and medical or other equipment for life support.

ADI assumes no responsibility for any damage resulting from the use of the LCD product in disregard of the conditions and handling precautions in this specification.

If customers intend to use the LCD product for the above items or other no standard items, please contact our sales persons in advance.

## 2. ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	MIN.	MAX.	UNIT
Power Supply Voltage for LCD	VCC	0	7.0	V
Logic Input Voltage	VI	-0.5	6.1	V
Operation Temperature *1)	T <sub>op</sub>	0	50	°C
Storage Temperature *1)	T <sub>stg</sub>	-20	60	°C

[Note]

\*1) T<sub>op</sub>, T<sub>stg</sub> ≤ 40°C : 90%RH max. without condensation

T<sub>op</sub>, T<sub>stg</sub> > 40°C : Absolute humidity shall be less than the value of 90%RH at 40 °C without condensation.

## 3. ELECTRICAL CHARACTERISTICS

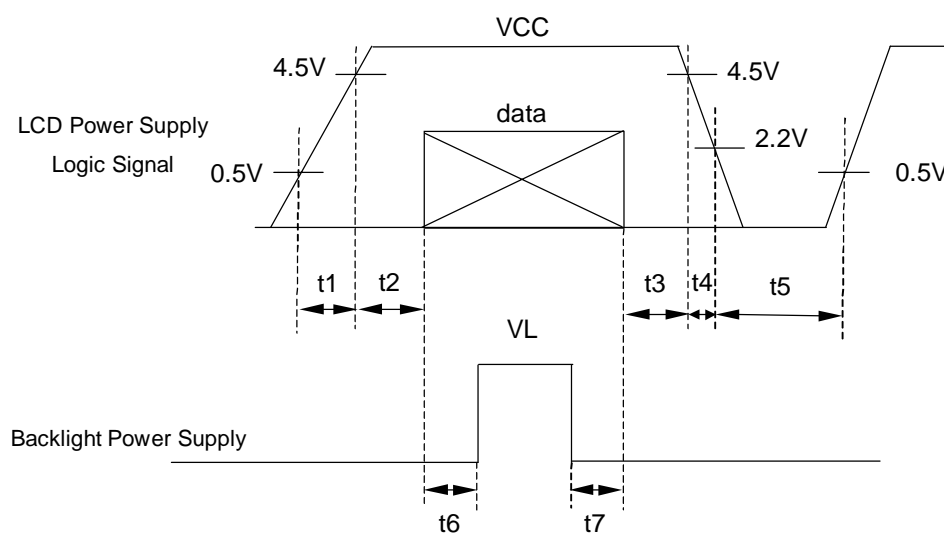
(1) TFT- LCD

T<sub>a</sub>=25°C

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	Remarks
Power Supply Voltages for LCD	VCC	4.5	5.0	5.5	V	*1)
Power Supply Currents for LCD	ICC	--	300	500	mA	*2)
Permissive Input Ripple Voltage	VRP	--	--	100	mVp-p	VCC = +5.0V
Logic Input Voltage	High	VIH	2.2	3.3	5.5	V
	Low	VIL	0	--	0.8	V

\*1) Power and signals sequence:

$$\begin{array}{ll}
 t_1 \leq 10\text{ms} & 1\text{sec} \leq t_5 \\
 0 < t_2 \leq 10\text{ms} & 200\text{ms} \leq t_6 \\
 0 < t_3 \leq 1\text{sec} & 0 \leq t_7 \\
 0 < t_4 \leq 50\text{ms} &
 \end{array}$$

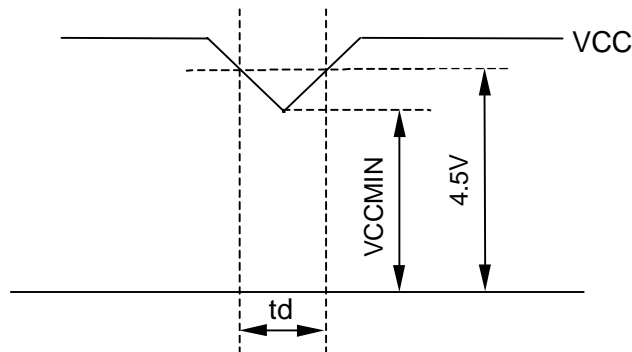


Data: RGB DATA, DCLK, HD, VD, DENA

VCC-dip conditions:

- 1) When  $V_{CCMIN} \geq 3.6\text{ V}$ ,  $t_d \leq 10\text{ ms}$
- 2) When  $V_{CCMIN} < 3.6\text{ V}$

VCC-dip conditions should also follow the power and signals sequence.



\*2) Typical current condition:

256- gray- bar-pattern

768 line mode

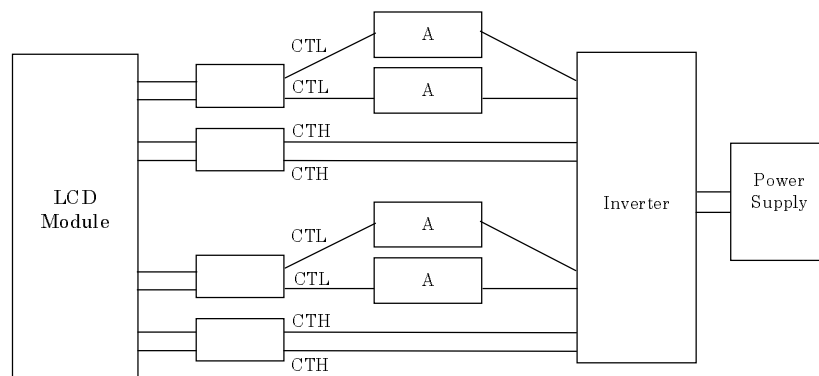
$V_{CC} = 5.0\text{V}$ ,  $f_H=48.4\text{kHz}$ ,  $f_V=60\text{Hz}$ ,  $f_{CLK}= 32.5\text{MHz}$

(2) Backlight

$T_a=25^\circ\text{C}$

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	Remarks
Lamp Voltage	VL	--	570	--	V	$I_L = 6.0\text{mA}$
Lamp Current	IL	3.5	6.0	8.0	mA	*1)
Lamp Frequency	FL	40	--	70	kHz	*2)
Starting Lamp Voltage	VS	1400	--	--	V	$T_a=0^\circ\text{C}$
		1200	--	--	V	$T_a=25^\circ\text{C}$
Lamp Life Time	LT	--	50000	--	h	*3), $I_L=6.0\text{mA}$ , Continuous Operation

\*1) Lamp Current measurement method (The current meter is inserted in low voltage line.)



\*2) Lamp frequency of inverter may produce interference with horizontal synchronous frequency, and this may cause horizontal beat on the display. Therefore, please adjust lamp frequency, and keep inverter as far from module as possible or use electronic shielding between inverter and module to avoid the interference.

\*3) Lamp life time is defined as the time either when the brightness becomes 50% of the initial value, or when the starting lamp voltage does not meet the value specified in this table.

## 4. INTERFACE PIN CONNECTION

### (1) CN 1(Data Signal and Power Supply)

Used Connector: IL-FHR-BF40S-HF (JAE)

Pin No.	Symbol	Function
1	GND	
2	VCC	
3	VCC	
4	RO0	Red odd data(LSB)
5	RO1	Red odd data
6	RO2	Red odd data
7	RO3	Red odd data
8	GND	
9	RO4	Red odd data
10	RO5	Red odd data
11	RO6	Red odd data
12	RO7	Red odd data(MSB)
13	GND	
14	GO0	Green odd data(LSB)
15	GO1	Green odd data
16	GO2	Green odd data
17	GO3	Green odd data
18	GND	
19	GO4	Green odd data
20	GO5	Green odd data
21	GO6	Green odd data
22	GO7	Green odd data(MSB)
23	GND	
24	BO0	Blue odd data(LSB)
25	BO1	Blue odd data
26	BO2	Blue odd data
27	BO3	Blue odd data
28	GND	
29	BO4	Blue odd data
30	BO5	Blue odd data
31	BO6	Blue odd data
32	BO7	Blue odd data(MSB)
33	GND	
34	NC	This pin should be open or GND.
35	HD	Horizontal Sync
36	VD	Vertical Sync
37	DENA	Data enable
38	GND	
39	DCLK	Dot Clock
40	GND	

(2) CN 2 (Data signal)

Used Connector: IL-FHR-BF36S-HF (JAE)

Pin No.	Symbol	Function
1	GND	
2	TEST	This pin should be open. Test signal output for only internal test use.
3	TEST	This pin should be open. Test signal output for only internal test use.
4	TEST	This pin should be open. Test signal output for only internal test use.
5	GND	
6	GND	
7	RE0	Red even data(LSB)
8	RE1	Red even data
9	RE2	Red even data
10	RE3	Red even data
11	GND	
12	RE4	Red even data
13	RE5	Red even data
14	RE6	Red even data
15	RE7	Red even data(MSB)
16	GND	
17	GE0	Green even data(LSB)
18	GE1	Green even data
19	GE2	Green even data
20	GE3	Green even data
21	GND	
22	GE4	Green even data
23	GE5	Green even data
24	GE6	Green even data
25	GE7	Green even data(MSB)
26	GND	
27	BE0	Blue even data(LSB)
28	BE1	Blue even data
29	BE2	Blue even data
30	BE3	Blue even data
31	GND	
32	BE4	Blue even data
33	BE5	Blue even data
34	BE6	Blue even data
35	BE7	Blue even data(MSB)
36	GND	

(3) CN 3, 4(Backlight)

Backlight-side connector: BHSR-02VS-1(JST)

Inverter-side connector: SM02B-BHSS-1-TB

Pin No.	Symbol	Function
1, 2	CTH	VLH (High Voltage)

[Note] VLH-VLL=VL

(4) CN 5, 6(Backlight)

Backlight-side connector: BHR-02VS-1(JST)

Inverter-side connector: SM02(4.0)B-BHS-1-TB

Pin No.	Symbol	Function
1, 2	CTL	VLL (Low Voltage)

[Note] VLH-VLL=VL

## 5. INTERFACE TIMING

### (1) Timing Specifications

ITEM		SYMBOL	MIN.	TYP.	MAX.	UNIT
DCLK *1) *4)	Frequency	$f_{CLK}$	30	32.5	40	MHz
	Period	$t_{CLK}$	25.0	30.8	33.3	ns
	Low Width	$t_{WCL}$	8	--	--	ns
	High Width	$t_{WCH}$	8	--	--	ns
DATA *1) (R,G,B,DENA, HD, VD)	Set up time	$t_{DS}$	2.3	--	--	ns
	Hold time	$t_{DH}$	7.3	--	--	ns
DENA *3)	Horizontal Active Time	$t_{HA}$	512	512	512	$t_{CLK}$
	Horizontal Front Porch	$t_{HFP}$	0	12	--	$t_{CLK}$
	Horizontal Back Porch	$t_{HBP}$	6	148	--	$t_{CLK}$
	Vertical Active Time	$t_{VA}$	768	768	768	$t_H$
	Vertical Front Porch	$t_{VFP}$	0	3	--	$t_H$
	Vertical Back Porch	$t_{VBP}$	4	35	--	$t_H$
HD *2)*4)	Frequency	$f_H$	--	48.4	62.5	kHz
	Period	$t_H$	16	20.7	--	$\mu s$
	Low Width	$t_{WHL}$	1	68	--	$t_{CLK}$
VD *2)	Frequency	$f_V$	55	60	75	Hz
	Period	$t_V$	13.3	16.7	18.2	ms
	Low Width	$t_{WVL}$	1	6	--	$t_H$

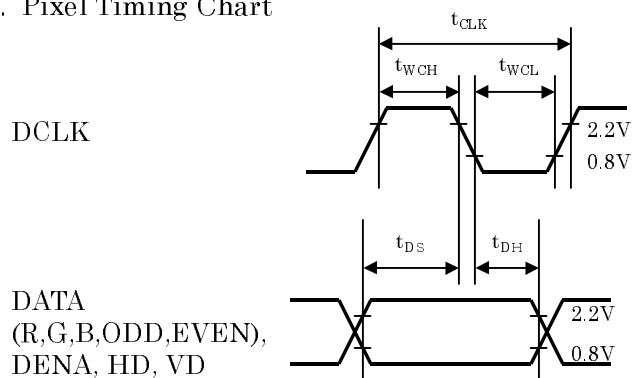
[Note]

- \*1) DATA is latched at fall edge of DCLK in this specification.
- \*2) Polarities of HD and VD are negative in this specification.
- \*3) DENA (Data Enable) should always be positive polarity as shown in the timing specification.
- \*4) DCLK should appear during all invalid period, and HD should appear during invalid period of frame cycle.

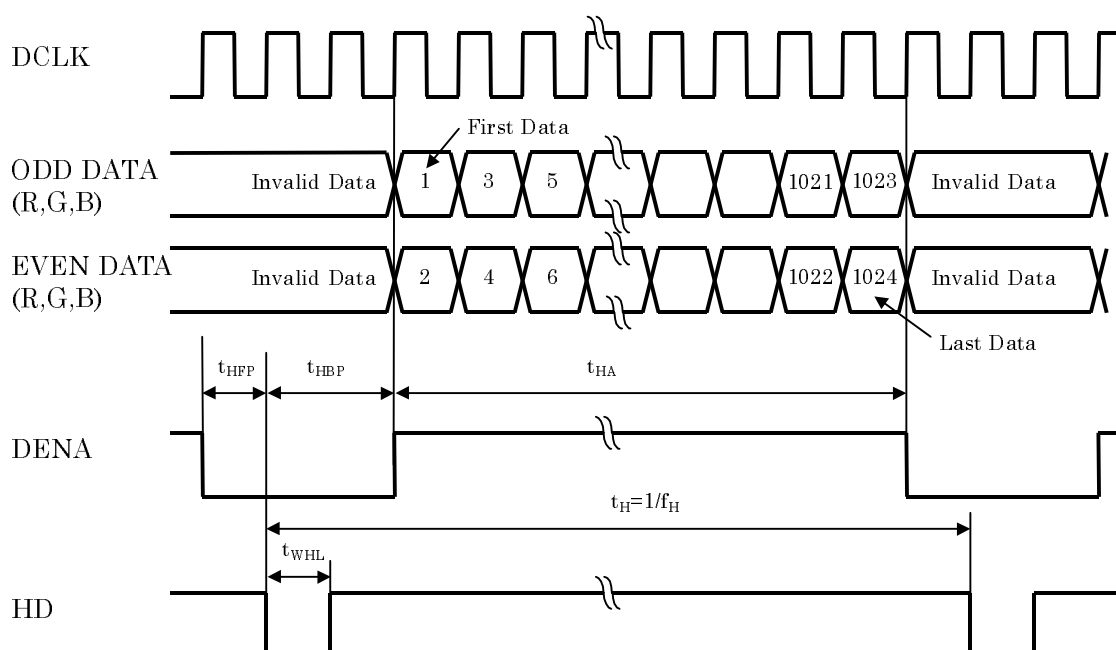


## (2) Timing Chart

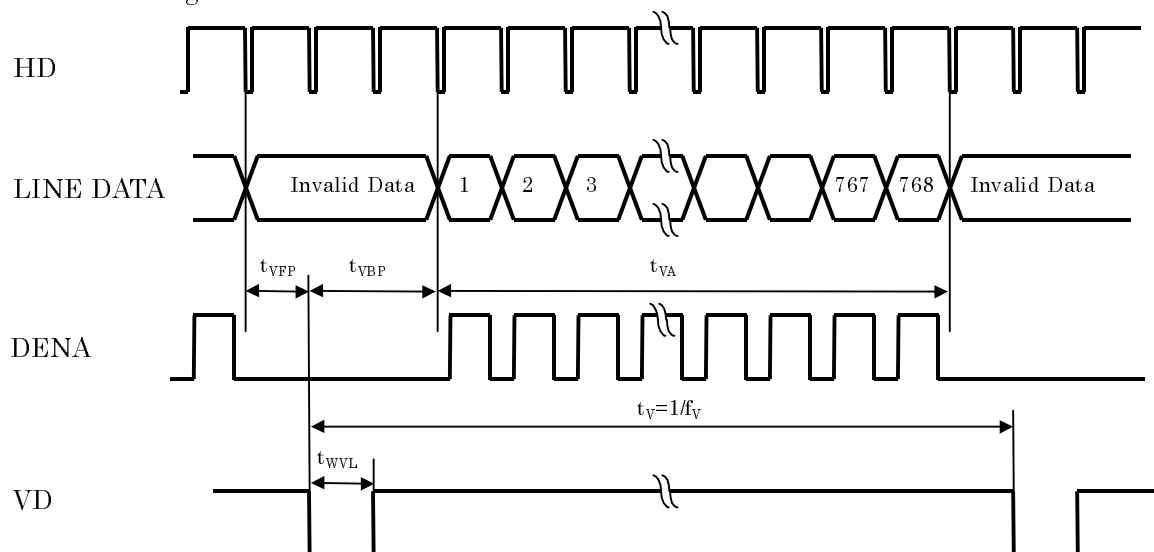
### a. Pixel Timing Chart



### b. Horizontal Timing Chart



### c. Vertical Timing Chart



### (3) Color Data Assignment

COLOR	INPUT DATA	R DATA								G DATA								B DATA							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
		MSB							LSB	MSB							LSB	MSB							LSB
BASIC COLOR	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	BLUE(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	CYAN	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	MAGENTA	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	YELLOW	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	WHITE	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
RED	RED(0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GREEN	GREEN(0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	GREEN(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	GREEN(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	GREEN(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
BLUE	BLUE(0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	BLUE(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	BLUE(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
	BLUE(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	BLUE(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

[Note]

\*1) Definition of gray scale

Color (n) ---n indicates gray scale level.

Higher n means brighter level.

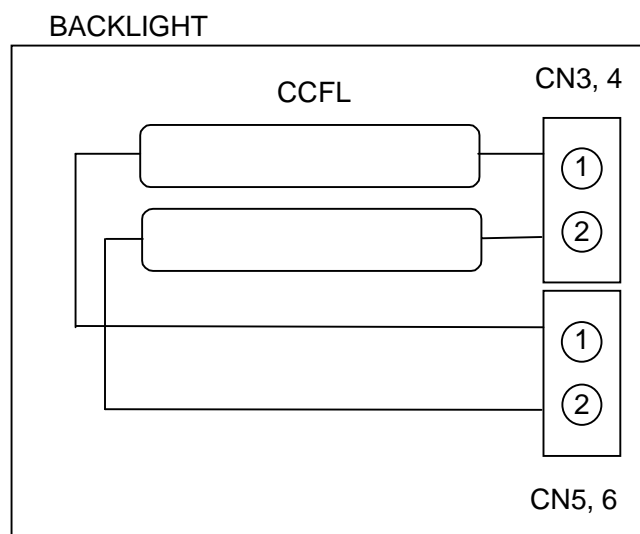
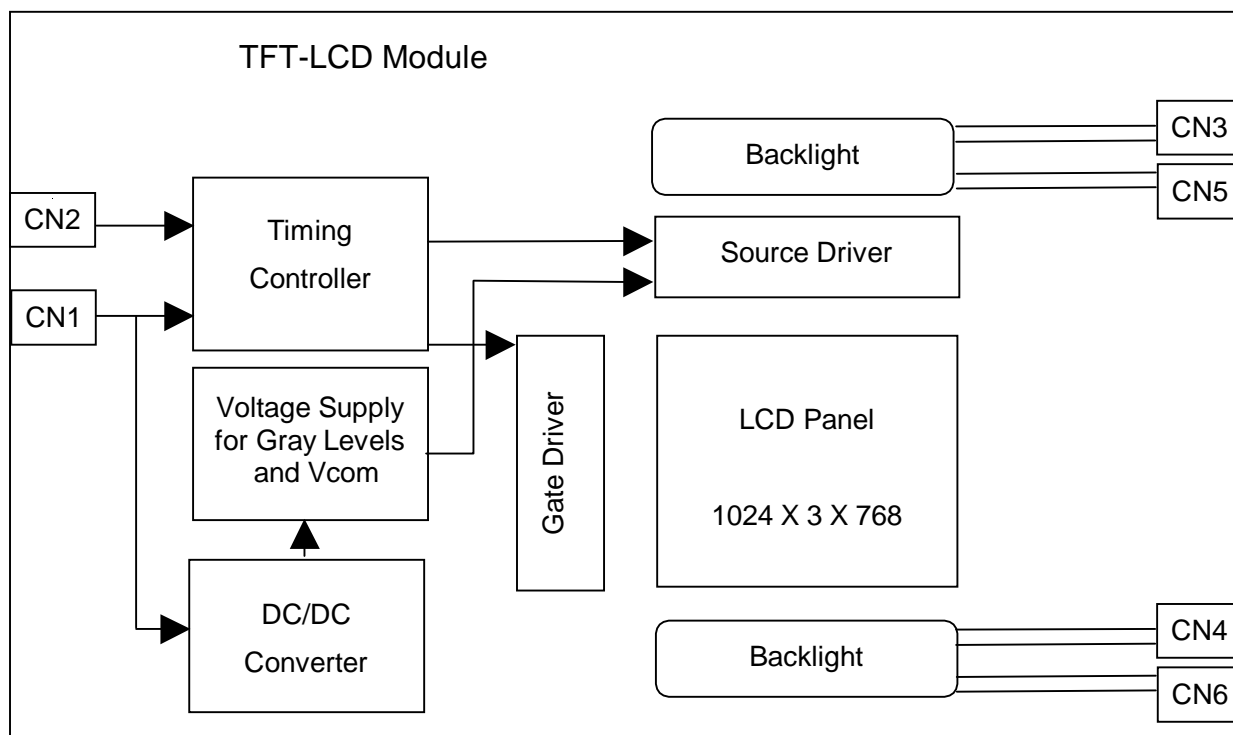
\*2) Data

1:High, 0: Low

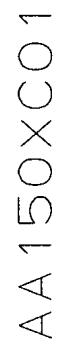
(4) Data Mapping

D( 1, 1)	D( 2, 1)	---	D( X, 1)	---	D(1023, 1)	D(1024, 1)
D( 1, 2)	D( 2, 2)	---	D( X, 2)	---	D(1023, 2)	D(1024, 2)
⋮	⋮	+	⋮	+	⋮	⋮
D( 1, Y)	D( 2, Y)	---	D( X, Y)	---	D(1023, Y)	D(1024, Y)
⋮	⋮	+	⋮	+	⋮	⋮
D( 1,767)	D( 2,767)	---	D( X,767)	---	D(1023,767)	D(1024,767)
D( 1,768)	D( 2,768)	---	D( X,768)	---	D(1023,768)	D(1024,768)

## 6. BLOCK DIAGLAM

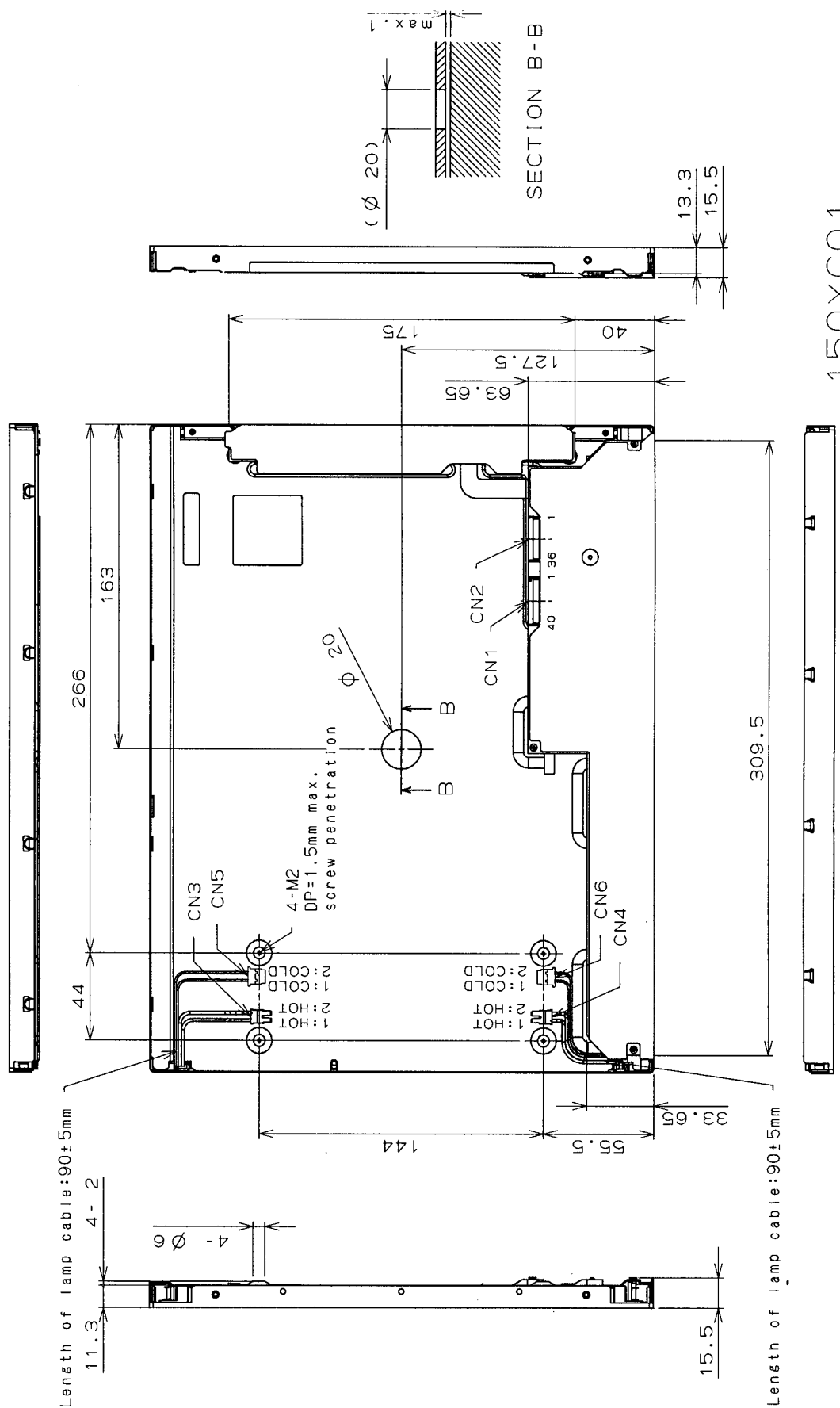


(1)Front side



1) Tolerance is  $\pm 0.5\text{mm}$  unless noted  
2) Except for thickness of PET film

(2)Rear side



1) Tolerance is ±0.5mm unless noted  
2) Except for thickness of PET film.

[Note]

We recommend you referring to the detailed drawing for your design.

Please contact our company sales representative when you need the detailed drawing.

## 8. OPTICAL CHARACTERISTICS

Ta=25°C, VCC=5.0V, Input Signals: Typ. Values shown in Section 5

ITEM		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	Remarks
Contrast Ratio		CR	$\theta = \phi = 0^\circ$	200	350	--	--	*1)*2)*3)
Luminance	Normal	Lw	$\theta = \phi = 0^\circ$	240	300	--	cd/m <sup>2</sup>	*2)*3)
	Uniformity	$\Delta Lw$	$\theta = \phi = 0^\circ$	--	--	30	%	*2)*3)
Response Time		tr	$\theta = \phi = 0^\circ$	--	6	--	ms	*3)*4)
		tf	$\theta = \phi = 0^\circ$	--	19	--	ms	*3)*4)
Viewing Angle	Horizontal	$\phi$	CR $\geq 10$	--	-75~75	--	°	*3)
	Vertical	$\theta$		--	-60~50	--	°	*3)
	Horizontal	$\phi$	CR $\geq 5$	--	-80~80	--	°	*3)
	Vertical	$\theta$		--	-80~70	--	°	*3)
Image Sticking		tis	2hours	--	--	2	s	*5)
Color Coordinates	Red	Rx	$\theta = \phi = 0^\circ$	0.605	0.635	0.665	--	*3)
		Ry		0.301	0.331	0.361		
	Green	Gx		0.253	0.283	0.313		
		Gy		0.561	0.591	0.621		
	Blue	Bx		0.109	0.139	0.169		
		By		0.022	0.052	0.082		
	White	Wx		0.273	0.303	0.333		
		Wy		0.283	0.313	0.343		

[Note]

These items are measured using CS1000(MINOLTA) for color coordinates, and CS1000 or BM-5A(TOPCON) for others under the dark room condition (no ambient light) after more than 30 minutes from turning on the lamp unless noted.

Condition: IL=6.0mA, Inverter frequency: 60kHz

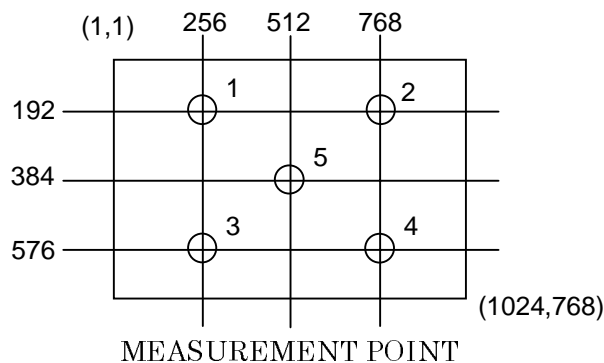
\*1) Definition of Contrast Ratio

CR=ON (White) Luminance / OFF(Black) Luminance

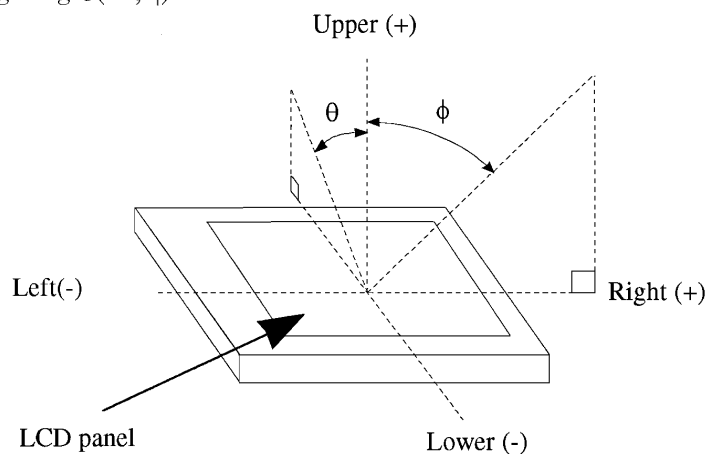
\*2) Definition of Contrast ratio, Luminance and Luminance Uniformity

$\Delta Lw = [Lw(\text{MAX})/Lw(\text{MIN}) - 1] \times 100$

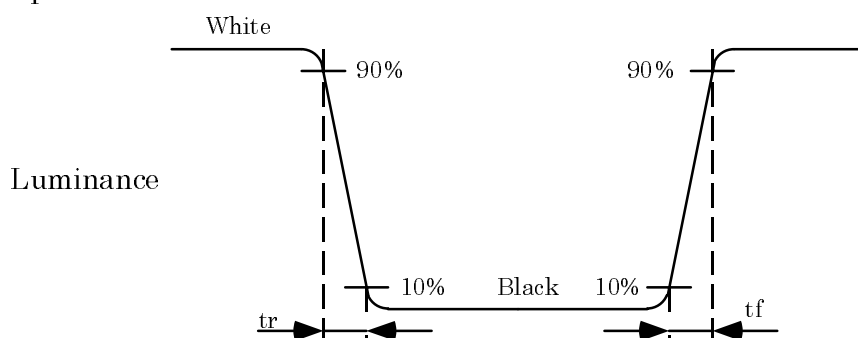
Measure Contrast ratio and White Luminance on the below 5 points



\*3) Definition of Viewing Angle(  $\theta$  ,  $\phi$  )

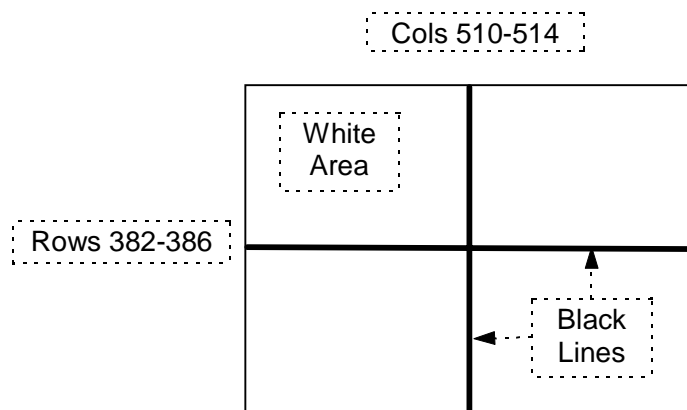


\*4) Definition of Response Time



\*5) Image Sticking

Continuously display the test pattern shown in the figure below for two-hours. Then display a completely white screen. The previous image shall not persist more than two seconds at 25°C.



TEST PATTERN FOR IMAGE STICKING TEST



## 9. RELIABILITY TEST CONDITION

### (1) Temperature and Humidity

TEST ITEM	CONDITIONS
HIGH TEMPERATURE HIGH HUMIDITY OPERATION	40°C, 90%RH, 240 h (No condensation)
HIGH TEMPERATURE OPERATION	50°C, 240 h
LOW TEMPERATURE OPERATION	0°C, 240 h
THERMAL SHOCK (Non-Operation)	BETWEEN -20°C (1h) and 60°C(1h), 5 CYCLES
HIGH TEMPERATURE STORAGE	60°C, 240 h
LOW TEMPERATURE STORAGE	-20°C, 240 h

### (2) Shock & Vibration

ITEM	CONDITIONS
SHOCK (NON-OPERATION)	Shock level: 980m/s <sup>2</sup> (100G) Waveform: half sinusoidal wave, 2ms Number of shocks: one shock input in each direction of three mutually perpendicular axes for a total of six shock inputs
VIBRATION (NON-OPERATION)	Vibration level: 9.8m/s <sup>2</sup> (1.0G) zero to peak Waveform: sinusoidal Frequency range: 5 to 500 Hz Frequency sweep rate: 0.5 octave /min Duration: one sweep from 5 to 500 to 5 Hz in each of three mutually perpendicular axis(each x,y,z axis: 1 hour, total 3 hours)

### (3) Judgment standard

The judgment of the above tests should be made as follow:

Pass: Normal display image with no obvious non-uniformity and no line defect.

Partial transformation of the module parts should be ignored.

Fail: No display image, obvious non-uniformity, or line defects.

## 10. HANDLING PRECAUTIONS FOR TFT-LCD MODULE

Please pay attention to the followings in handling TFT-LCD products;

### (1) ASSEMBLY PRECAUTION

- a. Please use the mounting hole on the module in installing and do not bending or wrenching LCD in assembling. And please do not drop, bend or twist LCD module in handling.
- b. Please design display housing in accordance with the following guide lines.
  - (a) Housing case must be designed carefully so as not to put stresses on LCD all sides and not to wrench module. The stresses may cause non-uniformity even if there is no non-uniformity statically.
  - (b) Keep sufficient clearance between LCD module back surface and housing when the LCD module is mounted. Approximately 1.0mm of the clearance in the design is recommended taking into account the tolerance of LCD module thickness and mounting structure height on the housing.
  - (c) When some parts, such as, FPC cable and ferrite plate, are installed underneath the LCD module, still sufficient clearance is required, such as 0.5mm. This clearance is, especially, to be reconsidered when the additional parts are implemented for EMI countermeasure.
  - (d) Design the inverter location and connector position carefully so as not to give stress to lamp cable, or not to interface the LCD module by the lamp cable.
  - (e) Keep sufficient clearance between LCD module and the others parts, such as inverter and speaker so as not to interface the LCD module. Approximately 1.0mm of the clearance in the design is recommended.
- c. Please do not push or scratch LCD panel surface with anything hard. And do not soil LCD panel surface by touching with bare hands. (Polarizer film, surface of LCD panel is easy to be flawed.)
- d. Please do not press any parts on the rear side such as source TCP, gate TCP, control circuit board and FPCs during handling LCD module. If pressing rear part is unavoidable, handle the LCD module with care not to damage them.
- e. Please wipe off LCD panel surface with absorbent cotton or soft cloth in case of it being soiled.
- f. Please wipe off drops of adhesives like saliva and water on LCD panel surface immediately. They might damage to cause panel surface variation and color change.
- g. Please do not take a LCD module to pieces and reconstruct it. Resolving and reconstructing modules may cause them not to work well.
- h. Please do not touch metal frames with bare hands and soiled gloves. A color change of the metal frames can happen during a long preservation of soiled LCD modules.
- i. Please pay attention to handling lead wire of backlight so that it is not tugged in connecting with inverter.
- j. Please connect the metal frame of LCD module to GND in order to minimize the effect of external

noise and EMI.

## **(2) OPERATING PRECAUTIONS**

- a. Please be sure to turn off the power supply before connecting and disconnecting signal input cable.
- b. Please do not change variable resistance settings in LCD module. They are adjusted to the most suitable value. If they are changed, it might happen LCD does not satisfy the characteristics specification.
- c. LCD backlight takes longer time to become stable of radiation characteristics in low temperature than in room temperature.
- d. A condensation might happen on the surface and inside of LCD module in case of sudden change of ambient temperature.
- e. Please pay attention not to display the same pattern for very long time. Image might stick on LCD. Even if image sticking happens, it may disappear as the operation time proceeds.
- f. Please obey the same safe instructions as ones being prepared for ordinary electronic products.

## **(3) PRECAUTIONS WITH ELECTROSTATICS**

- a. This LCD module use CMOS-IC on circuit board and TFT-LCD panel, and so it is easy to be affected by electrostatics. Please be careful with electrostatics by the way of your body connecting to the ground and so on.
- b. Please remove protection film very slowly from the surface of LCD module to prevent from electrostatics occurrence.

## **(4) STORAGE PRECAUTIONS**

- a. Please do not leave the LCDs in the environment of high humidity and high temperature such as 60°C90%RH.
- b. Please do not leave the LCDs in the environment of low temperature; below -20°C.

## **(5) SAFETY PRECAUTIONS**

- a. When you waste damaged or unnecessary LCDs, it is recommended to crush LCDs into pieces and wash them off with solvents such as acetone and ethanol, which should later be burned.
- b. If any liquid leaks out of a damaged glass cell and comes in contact with the hands, wash off thoroughly with soap and water.

## **(6) OTHERS**

- a. A strong incident light into LCD panel might cause display characteristics changing inferior because of polarizer film, color filter, and other materials becoming inferior. Please do not expose LCD module direct sunlight and strong UV rays.
- b. Please pay attention to a panel side of LCD module not to contact with other materials in preserving it alone.
- c. For the packaging box, please pay attention to the followings;
  - (a) Packaging box and inner case for LCD are designed to protect the LCDs from the damage or scratching during transportation. Please do not open except picking LCDs up from the box.
  - (b) Please do not pile them up more than 5 boxes. (They are not designed so.) And please do not turn over.
  - (c) Please handle packaging box with care not to give them sudden shock and vibrations. And also please do not throw them up.
  - (d) Packaging box and inner case for LCDs are made of cardboard. So please pay attention not to get them wet. (Such like keeping them in high humidity or wet place can occur getting them wet.)

# LCD Module Technical Specification

Aug 27, 2003  
Final Revision

\*\*\*\*\*

Type No.

**T-51511D150-FW-A-AD***I. Sato*

Approved by (Quality Assurance Division)

*H. Gondo*

Checked by (ACI Engineering Division)

*R. Wajuri*

Prepared by (Module Coordination Group)

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## 1. OVERVIEW

T-51511D150-FW-A-AD is 15.0" color TFT-LCD (Thin Film Transistor Liquid Crystal Display) modules composed of LCD panel, driver ICs, control circuit, and backlight unit.

By applying 8bit digital data,  $1024 \times 768$ , 16.7M-color images are displayed on the 15.0" diagonal screen. Input power voltages are 5.0 V for LCD driving.

The type of data and control signals are digital, and 2 pixel data are transmitted per Typ. 32.5 MHz clock cycle.

General specifications are summarized in the following table:

ITEM	SPECIFICATION
Display Area (mm)	304.1 (H) $\times$ 228.1 (V) (15.0-inch diagonal)
Number of Dots	$1024 \times 3$ (H) $\times$ 768 (V)
Pixel Pitch (mm)	0.297 (H) $\times$ 0.297 (V)
Color Pixel Arrangement	RGB vertical stripe
Display Mode	Normally white TN
Number of Color	16.7 M(8 bits/color)
Brightness	400 cd/m <sup>2</sup> (Typ.)
Wide Viewing Angle Technology	Optical Compensation Film
Viewing Angle (CR $\geq$ 10)	-75~75° (H) -60~50° (V)
Surface Treatment	Anti-glare and hard-coating 3H
Electrical Interface	CMOS(VI = 3~5 V, 2pixel / clock)
Optimum Viewing Angle(Contrast ratio)	6 o'clock
Module Size (mm)	326.0 (W) $\times$ 255.0 (H) $\times$ 15.5 (D)
Module Mass (g)	1390
Backlight Unit	CCFL, 4-tubes, edge-light

Characteristic value without any note is typical value.

The LCD product described in this specification is designed and manufactured for the standard use in OA equipment and consumer products, such as computers, communication equipment, industrial robots, AV equipment and so on.

Do not use the LCD product for the equipment that require the extreme high level of reliability, such as aerospace applications, submarine cables, nuclear power control systems and medical or other equipment for life support.

OPTREX assumes no responsibility for any damage resulting from the use of the LCD product in disregard of the conditions and handling precautions in this specification.

If customers intend to use the LCD product for the above items or other no standard items, please contact our sales persons in advance.

## 2. ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	MIN.	MAX.	UNIT
Power Supply Voltage for LCD	VCC	0	7.0	V
Logic Input Voltage	VI	-0.5	6.1	V
Lamp Voltage	VL	0	2500	V <sub>rms</sub>
Lamp Current	IL	0	10.0	mA <sub>rms</sub>
Lamp Frequency	FL	--	100	kHz
Operation Temperature *)	T <sub>op</sub>	0	50	°C
Storage Temperature *)	T <sub>stg</sub>	-20	60	°C

[Note]

\*) Top, Tstg ≤ 40°C : 90% RH max. without condensation

Top, Tstg > 40°C : Absolute humidity shall be less than the value of 90% RH at 40°C without condensation.

## 3. ELECTRICAL CHARACTERISTICS

(1) TFT- LCD

Ambient Temperature : Ta = 25°C

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	Remarks
Power Supply Voltages for LCD	VCC	4.5	5.0	5.5	V	*1)
Power Supply Currents for LCD	ICC	--	300	500	mA	*2)
Permissive Input Ripple Voltage	VRP	--	--	100	mVp-p	VCC = +5.0 V
Logic Input Voltage	High	VIH	2.2	3.3	V	
	Low	VIL	0	--	V	

\*1) Power and signals sequence:

$$t1 \leq 10 \text{ ms}$$

$$0 < t2 \leq 10 \text{ ms}$$

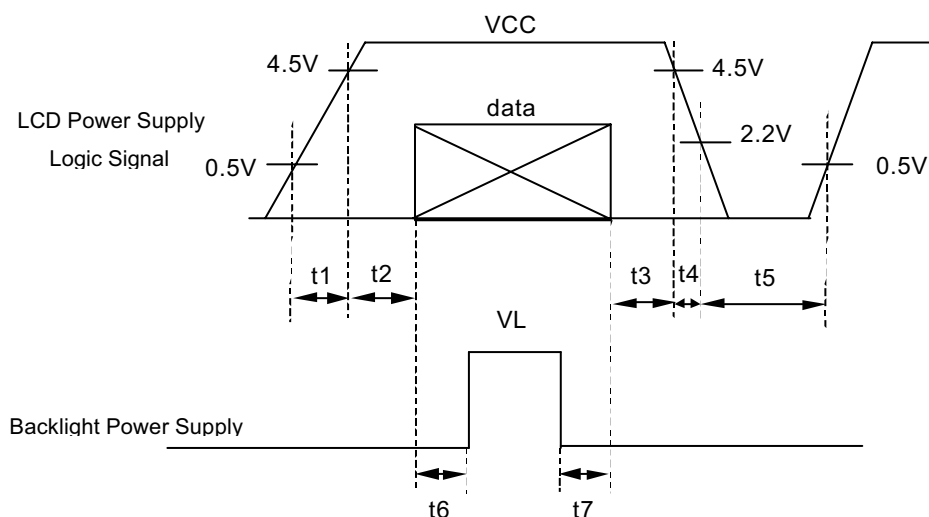
$$0 < t3 \leq 1 \text{ s}$$

$$0 < t4 \leq 50 \text{ ms}$$

$$1 \text{ s} \leq t5$$

$$200 \text{ ms} \leq t6$$

$$0 \leq t7$$

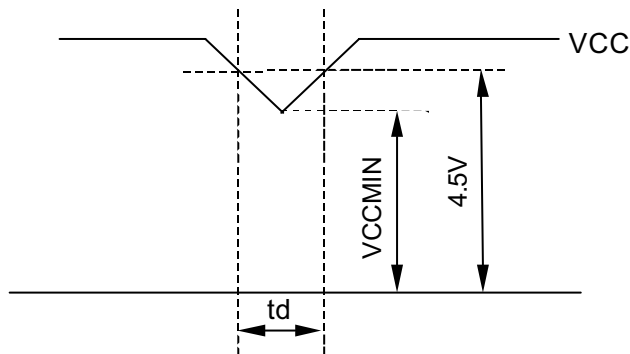


Data: RGB DATA. DCLK. HD. VD. DENA

VCC-dip conditions:

- 1) When  $VCC_{MIN} \geq 3.6\text{ V}$ ,  $t_d \leq 10\text{ ms}$
- 2) When  $VCC_{MIN} < 3.6\text{ V}$

VCC-dip conditions should also follow the power and signals sequence.



\*2) Typical current condition:

256- gray- bar-pattern

768 line mode

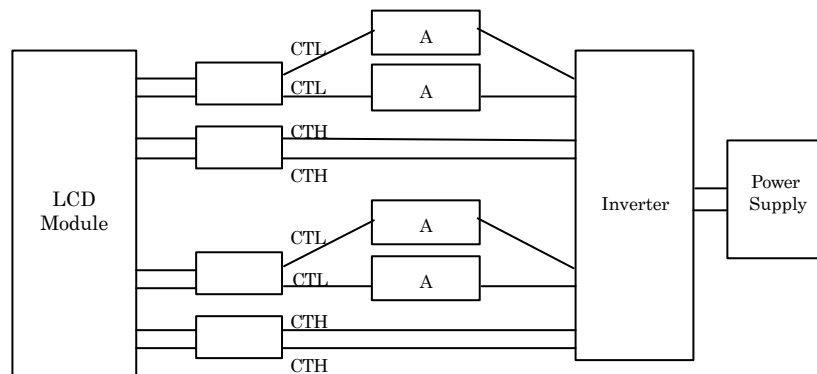
$VCC = 5.0\text{ V}$ ,  $f_H = 48.4\text{ kHz}$ ,  $f_V = 60\text{ Hz}$ ,  $f_{CLK} = 32.5\text{ MHz}$

(2) Backlight

$T_a = 25^\circ\text{C}$

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	Remarks
Lamp Voltage	VL	--	570	--	Vrms	$IL = 6.5\text{ mArms}$
Lamp Current	IL	3.5	6.5	8.0	mArms	*1)*4)
Lamp Frequency	FL	40	--	70	kHz	*2)
Starting Lamp Voltage	VS	1400	--	--	Vrms	$T_a = 0^\circ\text{C}$
		1200	--	--	Vrms	$T_a = 25^\circ\text{C}$
Lamp Life Time	LT	--	50000	--	h	*3), $IL = 6.5\text{ mArms}$ , Continuous Operation

\*1) Lamp Current measurement method (The current meter is inserted in low voltage line.)

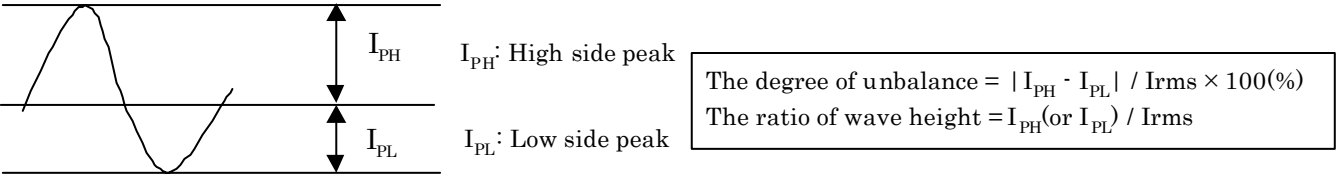


\*2) Lamp frequency of inverter may produce interference with horizontal synchronous frequency, and this may cause horizontal beat on the display. Therefore, please adjust lamp frequency, and keep inverter as far from module as possible or use electronic shielding between inverter and module to avoid the interference.

\*3) Lamp life time is defined as the time either when the brightness becomes 50% of the initial value, or when the starting lamp voltage does not meet the value specified in this table.



\*4) Please use the inverter which has symmetrical current wave form as follows,  
 The degree of unbalance: less than 10%  
 The ratio of wave height: less than  $\sqrt{2} \pm 10\%$



CURRENT WAVE FORM

## 4. INTERFACE PIN CONNECTION

(1) CN 1(Data Signal and Power Supply)

Used Connector: IL-FHR-BF40S-HF (JAE)

Pin No.	Symbol	Function
1	GND	
2	VCC	
3	VCC	
4	RO0	Red odd data(LSB)
5	RO1	Red odd data
6	RO2	Red odd data
7	RO3	Red odd data
8	GND	
9	RO4	Red odd data
10	RO5	Red odd data
11	RO6	Red odd data
12	RO7	Red odd data(MSB)
13	GND	
14	GO0	Green odd data(LSB)
15	GO1	Green odd data
16	GO2	Green odd data
17	GO3	Green odd data
18	GND	
19	GO4	Green odd data
20	GO5	Green odd data
21	GO6	Green odd data
22	GO7	Green odd data(MSB)
23	GND	
24	BO0	Blue odd data(LSB)
25	BO1	Blue odd data
26	BO2	Blue odd data
27	BO3	Blue odd data
28	GND	
29	BO4	Blue odd data
30	BO5	Blue odd data
31	BO6	Blue odd data
32	BO7	Blue odd data(MSB)
33	GND	
34	REV	Reverse scan control. L = Normal, H = Reverse
35	HD	Horizontal Sync
36	VD	Vertical Sync
37	DENA	Data enable
38	GND	
39	DCLK	Dot Clock
40	GND	

## (2) CN 2 (Data signal)

Used Connector: IL-FHR-BF36S-HF (JAE)

Pin No.	Symbol	Function
1	GND	
2	TEST	This pin should be open. Test signal output for only internal test use.
3	TEST	This pin should be open. Test signal output for only internal test use.
4	TEST	This pin should be open. Test signal output for only internal test use.
5	GND	
6	GND	
7	RE0	Red even data(LSB)
8	RE1	Red even data
9	RE2	Red even data
10	RE3	Red even data
11	GND	
12	RE4	Red even data
13	RE5	Red even data
14	RE6	Red even data
15	RE7	Red even data(MSB)
16	GND	
17	GE0	Green even data(LSB)
18	GE1	Green even data
19	GE2	Green even data
20	GE3	Green even data
21	GND	
22	GE4	Green even data
23	GE5	Green even data
24	GE6	Green even data
25	GE7	Green even data(MSB)
26	GND	
27	BE0	Blue even data(LSB)
28	BE1	Blue even data
29	BE2	Blue even data
30	BE3	Blue even data
31	GND	
32	BE4	Blue even data
33	BE5	Blue even data
34	BE6	Blue even data
35	BE7	Blue even data(MSB)
36	GND	

## (3) CN 3, 4(Backlight)

Backlight-side connector: BHSR-02VS-1(JST)

Inverter-side connector: SM02B-BHSS-1-TB

Pin No.	Symbol	Function
1, 2	CTH	VLH (High Voltage)

[Note] VLH-VBL = VL

## (4) CN 5, 6(Backlight)

Backlight-side connector: BHR-02VS-1(JST)

Inverter-side connector: SM02(4.0)B-BHS-1-TB

Pin No.	Symbol	Function
1, 2	CTL	VBL (Low Voltage)

[Note] VLH-VBL = VL

## 5. INTERFACE TIMING

### (1) Timing Specifications

ITEM		SYMBOL	MIN.	TYP.	MAX.	UNIT
DCLK *1) *4)	Frequency	$f_{CLK}$	30	32.5	40	MHz
	Period	$t_{CLK}$	25.0	30.8	33.3	ns
	Low Width	$t_{WCL}$	8	--	--	ns
	High Width	$t_{WCH}$	8	--	--	ns
DATA *1) (R,G,B,DENA, HD, VD)	Set up time	$t_{DS}$	2.3	--	--	ns
	Hold time	$t_{DH}$	7.3	--	--	ns
DENA *3)	Horizontal Active Time	$t_{HA}$	512	512	512	$t_{CLK}$
	Horizontal Front Porch	$t_{HFP}$	0	12	--	$t_{CLK}$
	Horizontal Back Porch	$t_{HBP}$	6	148	--	$t_{CLK}$
	Vertical Active Time	$t_{VA}$	768	768	768	$t_H$
	Vertical Front Porch	$t_{VFP}$	0	3	--	$t_H$
	Vertical Back Porch	$t_{VBP}$	4	35	--	$t_H$
HD *2)*4)	Frequency	$f_H$	--	48.4	62.5	kHz
	Period	$t_H$	16	20.7	--	$\mu s$
	Low Width	$t_{WHL}$	1	68	--	$t_{CLK}$
VD *2)	Frequency	$f_V$	55	60	75	Hz
	Period	$t_V$	13.3	16.7	18.2	ms
	Low Width	$t_{WVL}$	1	6	--	$t_H$

[Note]

\*1) DATA is latched at fall edge of DCLK in this specification.

\*2) Polarities of HD and VD are negative in this specification.

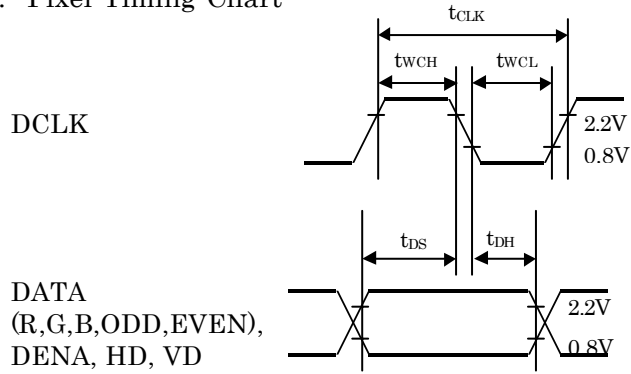
\*3) DENA (Data Enable) should always be positive polarity as shown in the timing specification.

\*4) DCLK should appear during all invalid period, and HD should appear during invalid period of frame cycle.

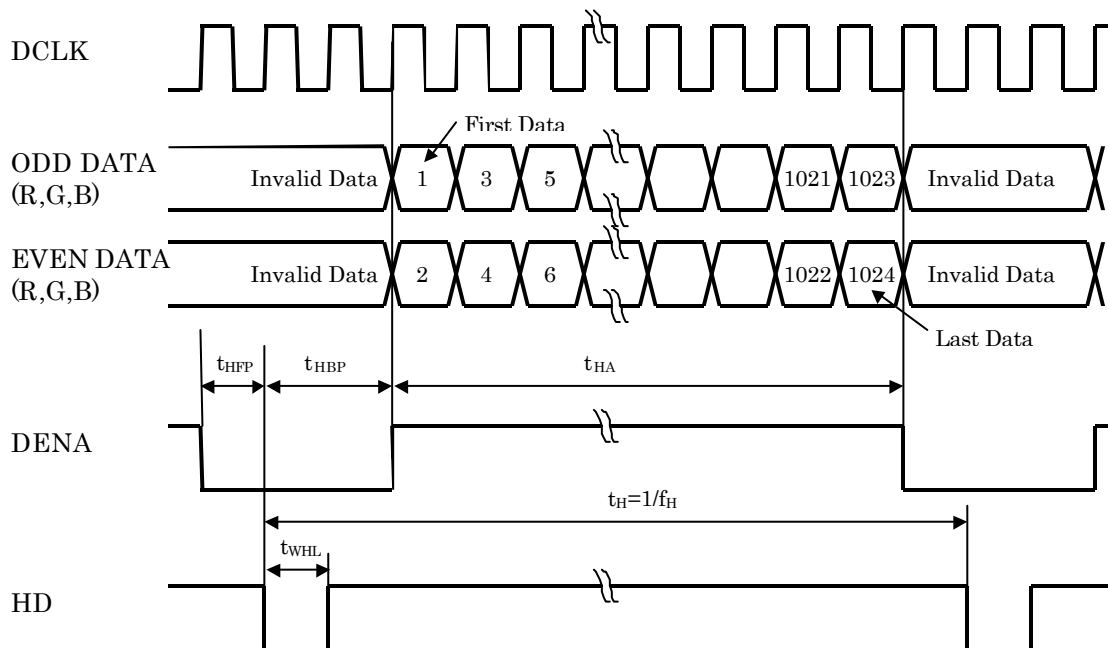
\*5)  $t_{HFP} + t_{HBP} \geq 85t_{CLK}$

## (2) Timing Chart

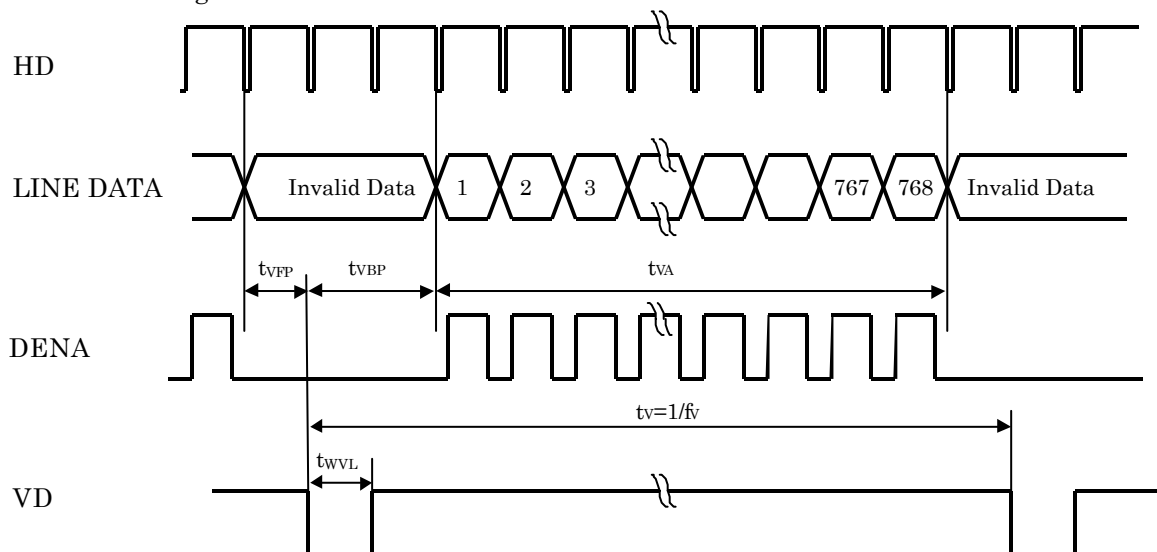
### a. Pixel Timing Chart



### b. Horizontal Timing Chart



### c. Vertical Timing Chart



### (3) Color Data Assignment

COLOR	INPUT DATA	R DATA								G DATA								B DATA							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
		MSB							LSB	MSB							LSB	MSB							LSB
BASIC COLOR	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	BLUE(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	CYAN	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	MAGENTA	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	YELLOW	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	WHITE	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
RED	RED(0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GREEN	GREEN(0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	GREEN(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	GREEN(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	GREEN(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
BLUE	BLUE(0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	BLUE(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	BLUE(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
	BLUE(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	BLUE(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

[Note]

\*1) Definition of gray scale

Color (n) --- n indicates gray scale level.

Higher n means brighter level.

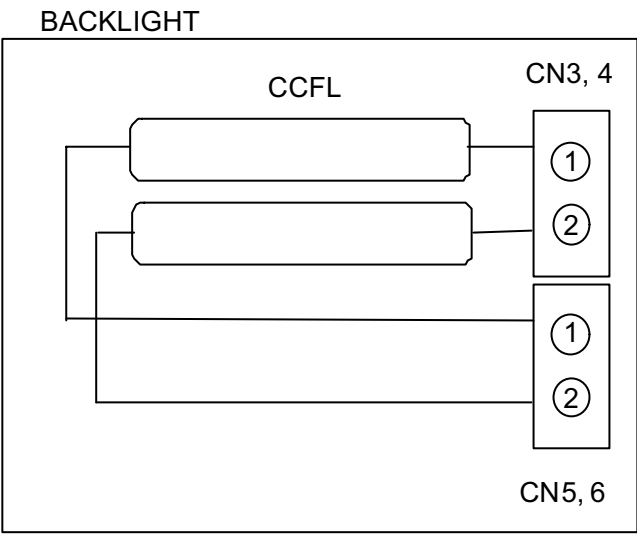
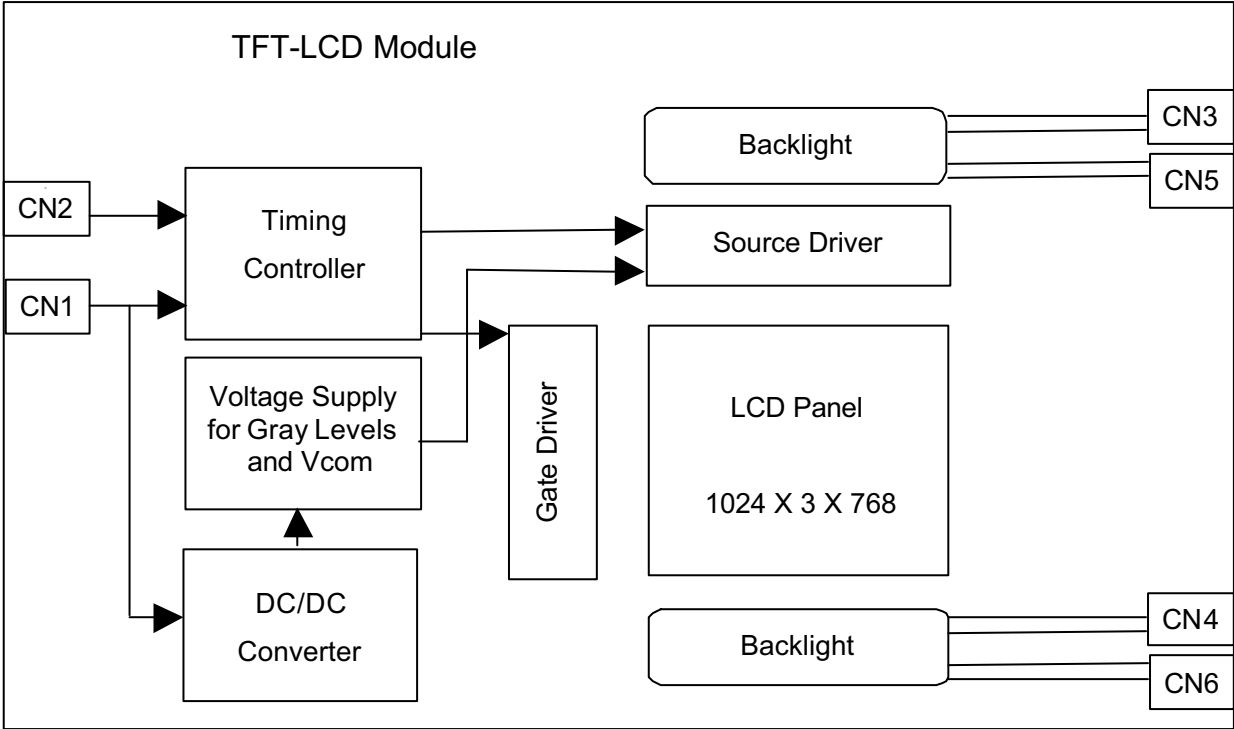
\*2) Data

1:High, 0: Low

(4) Data Mapping

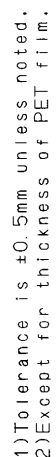
D( 1, 1)	D( 2, 1)	---	D( X, 1)	---	D(1023, 1)	D(1024, 1)
D( 1, 2)	D( 2, 2)	---	D( X, 2)	---	D(1023, 2)	D(1024, 2)
⋮	⋮	+	⋮	+	⋮	⋮
D( 1, Y)	D( 2, Y)	---	D( X, Y)	---	D(1023, Y)	D(1024, Y)
⋮	⋮	+	⋮	+	⋮	⋮
D( 1,767)	D( 2,767)	---	D( X,767)	---	D(1023,767)	D(1024,767)
D( 1,768)	D( 2,768)	---	D( X,768)	---	D(1023,768)	D(1024,768)

6. BLOCK DIAGRAM





(1)Front side



1) Tolerance is  $\pm 0.5$  mm unless noted.  
2) Except for thickness of PET film.  
\* 1: Two kinds of the products  
with and without this hole



We recommend you referring to the detailed drawing for your design.  
Please contact our company sales representative when you need the detailed drawing.

## 8. OPTICAL CHARACTERISTICS

Ta = 25°C, VCC = 5.0 V, Input Signals: Typ. Values shown in Section 5

ITEM		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	Remarks
Contrast Ratio		CR	$\theta = \phi = 0^\circ$	300	450	--	--	*1)*3)
Luminance	Normal	Lw	$\theta = \phi = 0^\circ$	320	400	--	cd/m <sup>2</sup>	*2)*3)
	Uniformity	$\Delta Lw$	$\theta = \phi = 0^\circ$	--	--	30	%	*2)*3)
Response Time		tr	$\theta = \phi = 0^\circ$	--	6	--	ms	*3)*4)
		tf	$\theta = \phi = 0^\circ$	--	19	--	ms	*3)*4)
Viewing Angle	Horizontal	$\phi$	CR $\geq 10$	--	-75~75	--	°	*3)
	Vertical	$\theta$		--	-60~50	--	°	*3)
	Horizontal	$\phi$	CR $\geq 5$	--	-80~80	--	°	*3)
	Vertical	$\theta$		--	-80~70	--	°	*3)
Image Sticking		tis	2 h	--	--	2	s	*5)
Color Coordinates	Red	Rx	$\theta = \phi = 0^\circ$	0.611	0.641	0.671	--	*3)
		Ry		0.304	0.334	0.364		
	Green	Gx		0.248	0.278	0.308		
		Gy		0.568	0.598	0.628		
	Blue	Bx		0.113	0.143	0.173		
		By		0.026	0.056	0.086		
	White	Wx		0.277	0.307	0.337		
		Wy		0.290	0.320	0.350		

[Note]

These items are measured using CS1000(MINOLTA) for color coordinates, EZContrast(ELDIM) for viewing angle and CS1000 or BM-5A(TOPCON) for others under the dark room condition (no ambient light) after more than 30 minutes from turning on the lamp unless noted.

Condition: IL = 6.5 mArms, Inverter frequency: 60 kHz

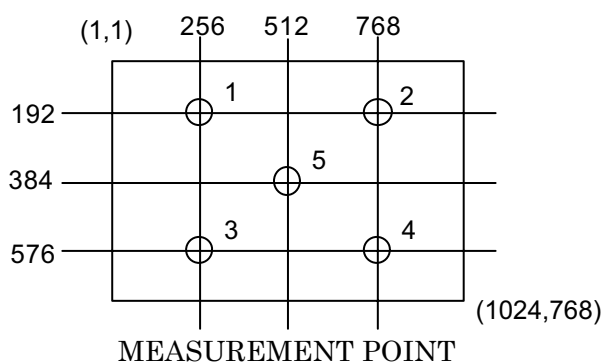
\*1) Definition of Contrast Ratio

CR=ON (White) Luminance / OFF(Black) Luminance: average of 5 points shown in a figure below

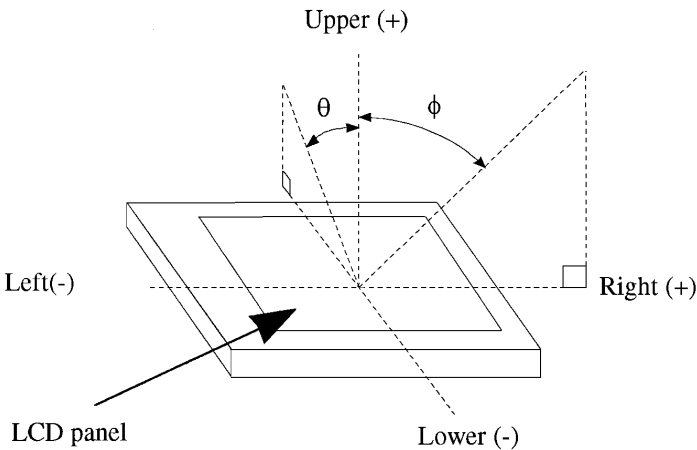
\*2) Definition of Luminance and Luminance Uniformity

Lw=ON (White) Luminance: average of 5 points shown in a figure below

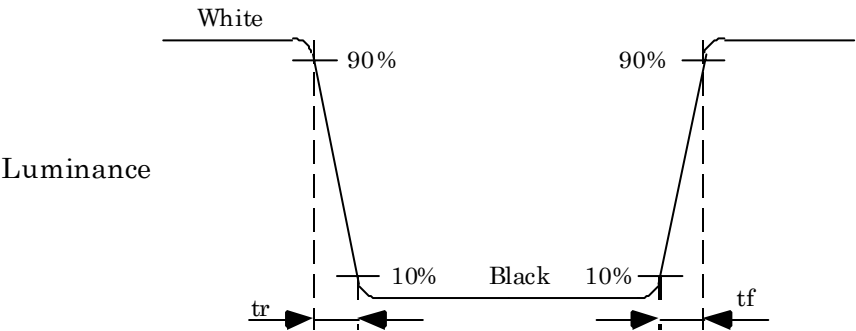
$\Delta Lw = [Lw(\text{MAX})/Lw(\text{MIN}) - 1] \times 100$



\*3) Definition of Viewing Angle(  $\theta$  ,  $\phi$  )

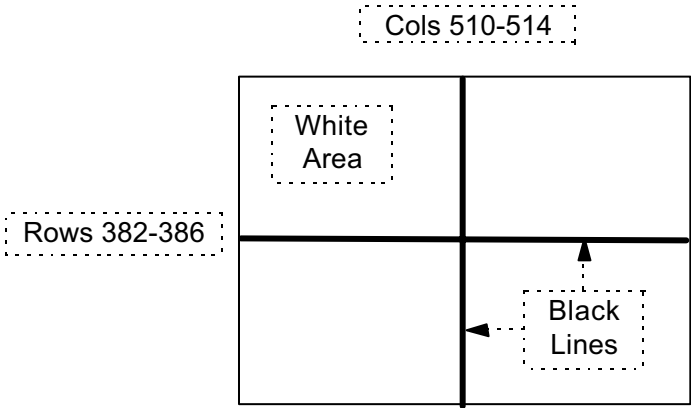


\*4) Definition of Response Time



\*5) Image Sticking

Continuously display the test pattern shown in the figure below for two-hours. Then display a completely white screen. The previous image shall not persist more than two seconds at 25°C.



TEST PATTERN FOR IMAGE STICKING TEST

## 9. RELIABILITY TEST CONDITION

### (1) Temperature and Humidity

TEST ITEM	CONDITIONS
HIGH TEMPERATURE HIGH HUMIDITY OPERATION	40°C, 90% RH, 240 h (No condensation)
HIGH TEMPERATURE OPERATION	50°C, 240 h
LOW TEMPERATURE OPERATION	0°C, 240 h
THERMAL SHOCK (Non-Operation)	BETWEEN -20°C (1h) and 60°C(1h), 5 CYCLES
HIGH TEMPERATURE STORAGE	60°C, 240 h
LOW TEMPERATURE STORAGE	-20°C, 240 h

### (2) Shock & Vibration

ITEM	CONDITIONS
SHOCK (NON-OPERATION)	Shock level: 980 m/s <sup>2</sup> (100 G) Waveform: half sinusoidal wave, 2 ms Number of shocks: one shock input in each direction of three mutually Perpendicular axes for a total of six shock inputs
VIBRATION (NON-OPERATION)	Vibration level: 9.8 m/s <sup>2</sup> (1.0 G)zero to peak Waveform: sinusoidal Frequency range: 5 to 500 Hz Frequency sweep rate: 0.5 octave /min Duration: one sweep from 5 to 500 Hz in each of three mutually perpendicular axis(each x,y,z axis: 1 hour, total 3 hours)

### (3) Judgment standard

The judgment of the above tests should be made as follow:

Pass: Normal display image with no obvious non-uniformity and no line defect.

Partial transformation of the module parts should be ignored.

Fail: No display image, obvious non-uniformity, or line defects.

## 10. INSPECTION STANDARDS

Inspection condition is as follows:

Viewing distance is approximately 35 cm.

Viewing angle is normal to the LCD panel.

Ambient temperature is approximately 25°C.

Ambient light is from 300 to 500 lx.

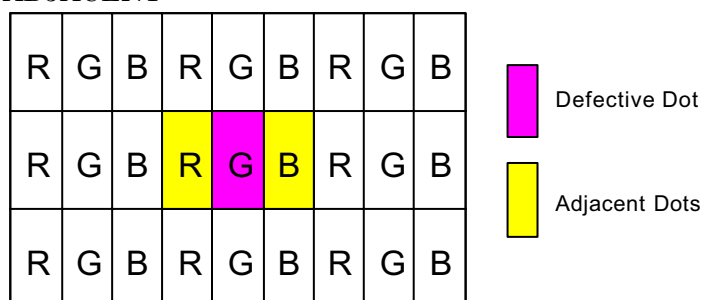
Bright Dot is defined as follows:

Visible through 5% transmission ND filter under the condition that black image (color 0) is on the display.

DEFECT TYPE		LIMIT	
VISUAL DEFECT	SCRATCH	$0.01 \text{ mm} < W \leq 0.05 \text{ mm}$ $L \leq 10 \text{ mm}$	$N \leq 4$
		$0.01 \text{ mm} < W$ $10 \text{ mm} < L$	$N = 0$
		$0.05 \text{ mm} < W$	$N = 0$
	DENT	$0.2 \text{ mm} < \phi \leq 0.4 \text{ mm}$	$N \leq 4$
		$0.4 \text{ mm} < \phi$	$N = 0$
	BLACK SPOT BUBBLE	$0.2 \text{ mm} < \phi \leq 0.4 \text{ mm}$	$N \leq 5$
		$0.4 \text{ mm} < \phi$	$N = 0$
	LINT	$L \leq 3 \text{ mm}$ $W \leq 0.1 \text{ mm}$	$N \leq 4$
		$3 \text{ mm} < L$ $W \leq 0.1 \text{ mm}$	$N = 0$
		$0.1 \text{ mm} < W$	ACCORDING TO BLACK SPOT
ELECTRICAL DEFECT	BRIGHT DOT	$N \leq 5$	
	DARK DOT	$N \leq 5$	
	TOTAL DOT	$N \leq 8$	
	TWO ADJACENT DOT BRIGHT DOT DARK DOT	$\leq 2 \text{ PAIRS}$ $\leq 2 \text{ PAIRS}$	
	THREE OR MORE ADJACENT DOT	NOT ALLOWED	
	DISTANCE BETWEEN DEFECTS BRIGHT DOT DARK DOT	$\geq 15 \text{ mm}$ $\geq 15 \text{ mm}$	
	LINE DEFECT	NOT ALLOWED	

\*1) W: width, L: length,  $\phi$ : diameter, N: number

\*2) DEFINITION OF ADJACENT



The defects that are not defined above and considered to be problem shall be reviewed and discussed by both parties.

## 11. HANDLING PRECAUTIONS FOR TFT-LCD MODULE

Please pay attention to the followings in handling TFT-LCD products;

### (1) ASSEMBLY PRECAUTION

- a. Please mount the LCD module by using mounting hole with a screw clamping torque less than 0.5 Nm. Please do not bend or wrench the LCD module in assembling. Please do not drop, bend or twist the LCD module in handling. Please mount the inverter circuit board by using mounting hole of rear side with a screw clamping torque less than 0.2 Nm.
- b. Please design display housing in accordance with the following guide lines.
  - (a) Housing case must be designed carefully so as not to put stresses on LCD all sides and not to wrench module. The stresses may cause non-uniformity even if there is no non-uniformity statically.
  - (b) Keep sufficient clearance between LCD module back surface and housing when the LCD module is mounted. Approximately 1.0mm of the clearance in the design is recommended taking into account the tolerance of LCD module thickness and mounting structure height on the housing.
  - (c) When some parts, such as, FPC cable and ferrite plate, are installed underneath the LCD module, still sufficient clearance is required, such as 0.5mm. This clearance is, especially, to be reconsidered when the additional parts are implemented for EMI countermeasure.
  - (d) Design the inverter location and connector position carefully so as not to give stress to lamp cable, or not to interface the LCD module by the lamp cable.
  - (e) Keep sufficient clearance between LCD module and the others parts, such as inverter and speaker so as not to interface the LCD module. Approximately 1.0mm of the clearance in the design is recommended.
- c. Please do not push or scratch LCD panel surface with anything hard. And do not soil LCD panel surface by touching with bare hands. (Polarizer film, surface of LCD panel is easy to be flawed.)
- d. Please do not press any parts on the rear side such as source TCP, gate TCP, control circuit board and FPCs during handling LCD module. If pressing rear part is unavoidable, handle the LCD module with care not to damage them.
- e. Please wipe off LCD panel surface with absorbent cotton or soft cloth in case of it being soiled.
- f. Please wipe off drops of adhesives like saliva and water on LCD panel surface immediately. They might damage to cause panel surface variation and color change.
- g. Please do not take a LCD module to pieces and reconstruct it. Resolving and reconstructing modules may cause them not to work well.
- h. Please do not touch metal frames with bare hands and soiled gloves. A color change of the metal frames can happen during a long preservation of soiled LCD modules.
- i. Please pay attention to handling lead wire of backlight so that it is not tugged in connecting with

inverter.

- j. Please connect the metal frame of LCD module to GND in order to minimize the effect of external noise and EMI.
- k. Be sure to connect the cables and the connectors correctly.

## **(2) OPERATING PRECAUTIONS**

- a. Please be sure to turn off the power supply before connecting and disconnecting signal input cable.
- b. Please do not change variable resistance settings in LCD module. They are adjusted to the most suitable value. If they are changed, it might happen LCD does not satisfy the characteristics specification.
- c. LCD backlight takes longer time to become stable of radiation characteristics in low temperature than in room temperature.
- d. The interface signal speed is very high. Please pay attention to transmission line design and other high speed signal precautions to satisfy signal specification.
- e. A condensation might happen on the surface and inside of LCD module in case of sudden change of ambient temperature.
- f. Please pay attention not to display the same pattern for very long time. Image might stick on LCD. Even if image sticking happens, it may disappear as the operation time proceeds.
- g. Please obey the same safe instructions as ones being prepared for ordinary electronic products.

## **(3) PRECAUTIONS WITH ELECTROSTATICS**

- a. This LCD module use CMOS-IC on circuit board and TFT-LCD panel, and so it is easy to be affected by electrostatics. Please be careful with electrostatics by the way of your body connecting to the ground and so on.
- b. Please remove protection film very slowly from the surface of LCD module to prevent from electrostatics occurrence.

## **(4) STORAGE PRECAUTIONS**

- a. Please do not leave the LCDs in the environment of high humidity and high temperature such as 60°C/90% RH.
- b. Please do not leave the LCDs in the environment of low temperature; below -20°C.

## **(5) SAFETY PRECAUTIONS**

- a. When you waste damaged or unnecessary LCDs, it is recommended to crush LCDs into pieces and wash them off with solvents such as acetone and ethanol, which should later be burned.



- b. If any liquid leaks out of a damaged glass cell and comes in contact with the hands, wash off thoroughly with soap and water.
- c. Be sure to turn off the power supply when inserting or disconnecting the cable.
- d. Inverter should be designed carefully so as not to keep working in case of detecting over current or open circuit on the lamp.

## **(6) OTHERS**

- a. A strong incident light into LCD panel might cause display characteristics changing inferior because of polarizer film, color filter, and other materials becoming inferior. Please do not expose LCD module direct sunlight and strong UV rays.
- b. Please pay attention to a panel side of LCD module not to contact with other materials in preserving it alone.
- c. For the packaging box, please pay attention to the followings:
  - (a) Packaging box and inner case for LCD are designed to protect the LCDs from the damage or scratching during transportation. Please do not open except picking LCDs up from the box.
  - (b) Please do not pile them up more than 5 boxes. (They are not designed so.) And please do not turn over.
  - (c) Please handle packaging box with care not to give them sudden shock and vibrations. And also please do not throw them up.
  - (d) Packaging box and inner case for LCDs are made of cardboard. So please pay attention not to get them wet. (Such like keeping them in high humidity or wet place can occur getting them wet.)

## Packaging Specification

### 1. Packaging box

material:	cardboard
construction:	See fig. 1
max. packaging number:	10 pcs.
dimension:	488 (W) × 395 (H) × 361 (D)[mm]
mass(including 10 modules):	17.8 kg
label:	Labels are put on the box.(See fig. 2, 3, 4)

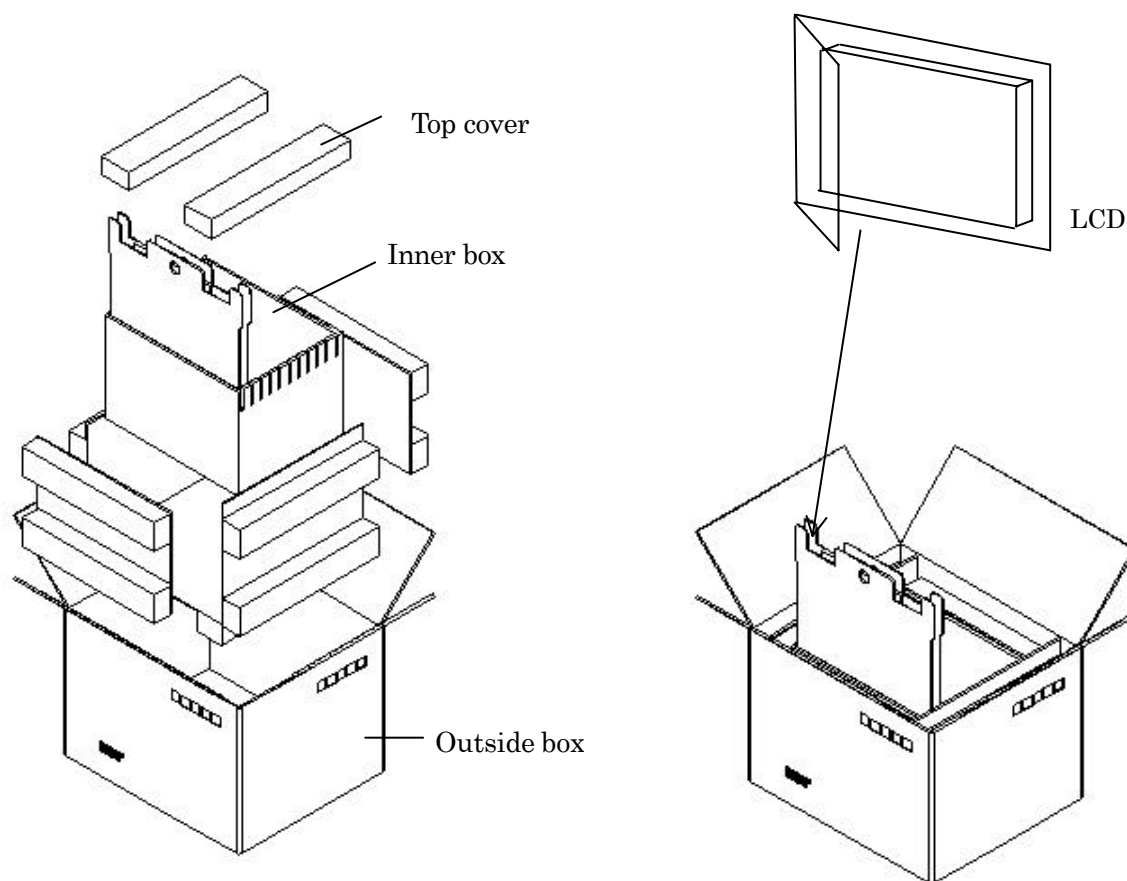


Fig. 1. Illustration of packaging box structure

Product name	Packaging number
Bar-code	Bar-code
Serial No.	Serial No.
Bar-code	Bar-code
Serial No.	Serial No.
Bar-code	Bar-code
Serial No.	Serial No.
Bar-code	Bar-code
Serial No.	Serial No.
Bar-code	Bar-code
Serial No.	Serial No.
Bar-code	Bar-code

Fig.2. Label1

Consignee
Product name
Product name of consignee
Order No.
Box No.
Place of production
Bar-code
Shipping date

Fig. 4. Label 3

Shipper	Box No.
	Mass
Shipping No.	
Bar-code	
Shipping No.	
Bar-code	
Packaging No.	
Bar-code	
Shipping No.	
Bar-code	
Products name	
Bar-code	

Fig.3. Label 2




OPTREX
TFT - LCD AA150XC01
T-51511D150-FW-A-AC
P / O NO. 123456789
C / S 001 OF 005
MADE IN JAPAN
<div>  001 </div> <div>  JA1BK4144 </div>
<div> 2001/11/15 </div> <div>  </div>

Fig. 5 Sample of Label3

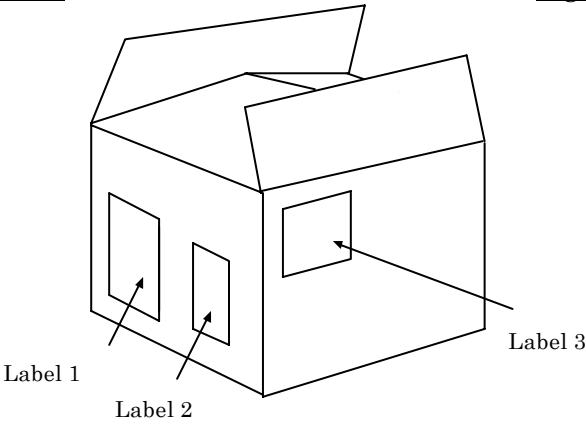


Fig. 6. Location of Labels

2. Location of label on the packaging box

- Labels are put on the box.(See Fig.6)

3. Packaging form of product

- Each of LCD module is packed in anti-electrostatic bag(Fig. 7)
- Packed LCD module is put in the packaging box.(Fig. 8)
- The packaging box accumulates maximum 10 modules.
- Upper protector is put on the products and shut the box.(Fig. 9)

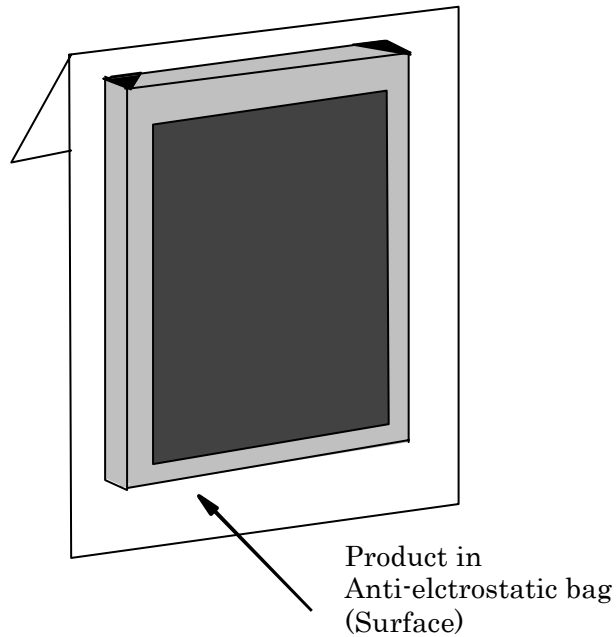


Fig. 7

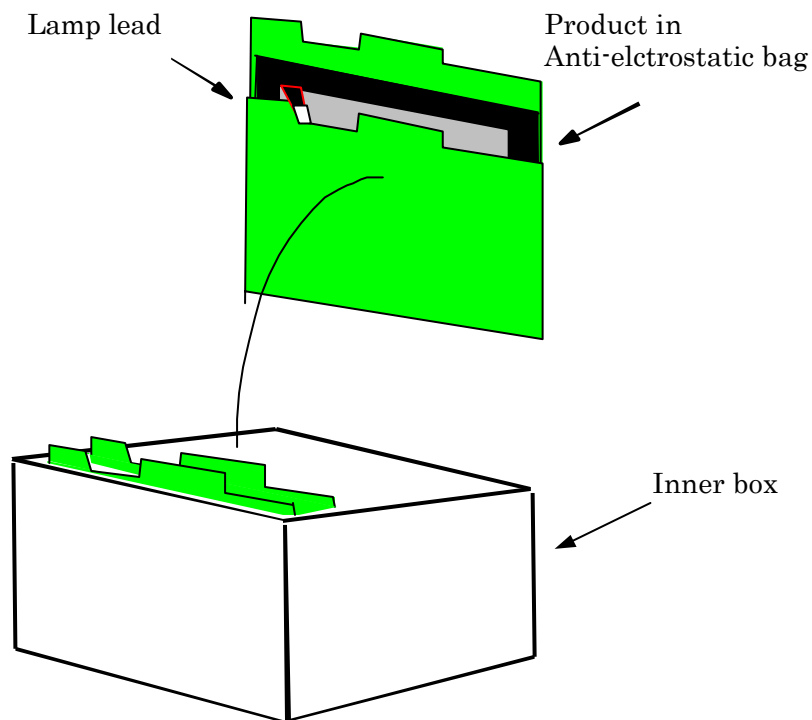


Fig. 8

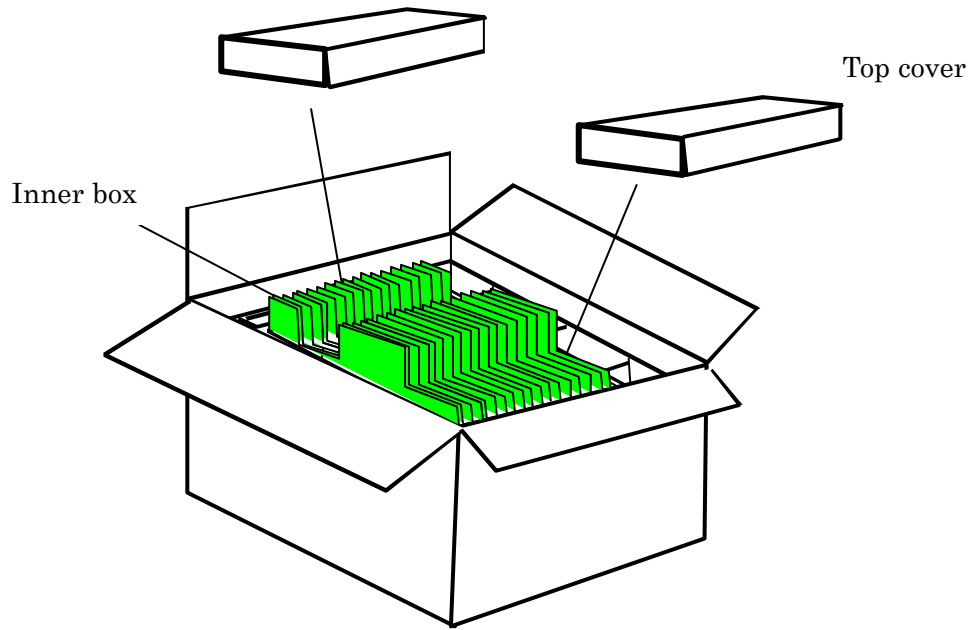


Fig. 9

#### 4. Cautions of shipping & storage

- Do not turn the packaging upside down while storage and transportation. The boxes should not be piled up more than 5.
- Handle with care. Keep off from rain & dew.
- Keep off from direct sunlight exposure. Please store under room temperature & low humidity in original packaging condition when they were shipped.
- Keep other cautions described in handling manual.

# Products Number Labeling Forms

Products number label is constructed as below;

① Brand Name, Symbol

② T-51512D121-FW-A-AA


③ AA121SK26

④ ABC1234567890


⑤ 60100001L

⑥ 

Bar-code



WARNING  
LAMP HIGH  
VOLTAGE

 ⑦ E158720 ⑧ Made in Japan

① Brand Name, Symbol

② Products Name of Optrex

③ Products Name

④ Production Key Number(13Digits)

⑤ Date Code  
(Serial Number, Factory Sign)

⑥ Bar-code of Date Code

⑦ UL File No.

⑧ Production Country

① Brand Name, Symbol  
OPTREX

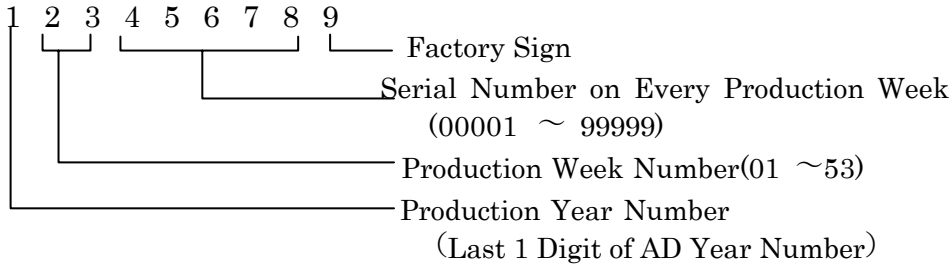
② Products Name of Optrex  
ex. T51512D121-FW-A-AA

③ Products Name  
ex.1: AA121SK26      ex.2: AA150XA03 B

④ Production Key Number(13Digits)  
(ID Number for Production Control)

⑤ Date Code (Serial Number, Factory Sign)

□ □ □ □ □ □ □ □ □



- Date Code is constructed by 9 Digits as below;  
1st Digit : Production Year Number (Last 1 Figure of AD Year)  
2nd~3rd Digit : Production Week Number in a Year  
(A Year is divided to 53 weeks from Monday to Saturday)  
4th~8th Digit : Serial Number on Every Production Weeks.  
( 00001 ~ 99999 )  
These are numbered in order according to Production Name.  
9th Digit : Factory Sign ( on the Module Test Process)  
( L: Shisui Factory Line, Y: YACHIYO SANYO Industries Line,  
W: CPT Fab-1, R: CPT Fab-2 , U: CPT Wujiang-LCM)

⑥Bar-code(Date Code)

Bar-code Line for computer reading Date Code mentioned as above.

⑦UL File No.

ADI: E158720, CPT: E194548

⑧Production Country

ADI: Made in Japan, CPT: Made in Taiwan

## LAMP UNIT for 15.0"XGA

### APPLICATION

This technical literature applies to the replaceable lamp unit that is the maintenance parts for 15.0"XGA TFT-LCD module industrial use(model name:T-51511D150-FW-A-AD).  
(AA-L5902086G01(Top), AA-L5902087G01(Bottom))

### MECHANICAL CHARACTERISTICS

Item	Specification	Remarks
Outline Dimension of Reflector	323.6±0.6 × 7.0±0.1 × 8.3±0.1(mm)	Except wire
Mass	22±3(g)(MAX)	With wire and connector
Lamp Diameter	φ 2.6-2.0 (mm)	

See DRAWING OF OUTLINE DIMENTIONS

### ENVIRONMENTAL CONDITIONS

Item	Operation		Non Operation		Remarks
	MIN	MAX	MIN	MAX	
Ambient Temperature	0°C	50°C	-25°C	60°C	No Condensation

Top,Tstg ≤ 40°C : 90%RH max. without condensation

Top,Tstg > 40°C : Absolute humidity shall be less than the value of 90%RH at 40°C without condensation.

### ABSOLUTE MAXIMUM RATINGS

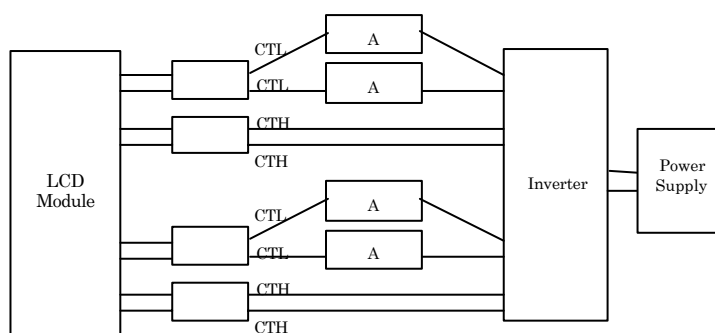
Item	Symbol	MIN	MAX	UNIT
Lamp Current	IL	0	10.0	mArms
Lamp Voltage	VL	0	2500	Vrms
Lamp Frequency	FL	0	100	kHz

### ELECTRICAL CHARACTERISTICS

Item	Symbol	Condition	MIN	TYP	MAX	Unit	Remarks
Lamp Current	IL	Ta = 25°C	3.5	6.5	8.0	mArm	
Lamp Voltage	VL	Ta = 25°C	-	570	-	Vrms	
Starting Lamp Voltage	VS	Ta = 25°C	1200	-	-	Vrms	
		Ta = 0°C	1400	-	-	Vrms	
Lamp Frequency	FL	Ta = 25°C, IL = 6.5 mArms	40	-	70	kHz	

\*1) These values are shown by ALPUS Electric using ALPS-UHP061095 inverter.

\*2) Lamp Current measurement method (The current meter is inserted in low voltage line.)





## OPTICAL CHARACTERISTICS

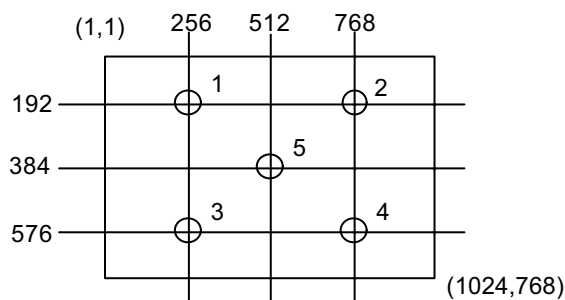
Ta=25°C, 60±10%RH

Item	Symbol	MIN	TYP	MAX	Unit	Remarks
Luminance	XC01	Lw	240	300	--	cd/m <sup>2</sup>
	XC03	Lw	320	400	--	cd/m <sup>2</sup>
Color Coordinates (White)	XC01	W <sub>x</sub>	0.273	0.303	0.333	-
		W <sub>y</sub>	0.283	0.313	0.343	-
	XC03	W <sub>x</sub>	0.277	0.307	0.337	-
		W <sub>y</sub>	0.290	0.320	0.350	-

[Conditions]

IL=6.5 mArms, Inverter frequency: 60kHz

[Measurement Point]



These items are measured when lamp units are assembled into T-51511D150-FW-A-AD, and using CS1000(MINOLTA) for color coordinates, and CS1000 or BM-5A(TOPCON) for others under the dark room condition (no ambient light) after more than 30 minutes from turning on the lamp unless noted.

## LIFE TIME OF THE LAMP UNIT

Environmental Conditions are as follows:

Ambient temperature is 25±5°C.

Lamp Current is 6.5 mArms.

Continuous Operation	50,000 h
Number of turning on and off	100,000 times (30 sec ON-OFF)

- (1) Lamp life time is defined as the time either when the brightness becomes 50% of the initial value, or when the starting lamp voltage does not meet the value specified in the table of section 4.
- (2) The life time of the backlight depends on the ambient temperature. The life time will decrease under low/high temperature.
- (3) Following standards should be satisfied
  - No flickers should be allowed.
  - Decrease in luminous length that is caused by lamp blacking is within 11 mm from the edge of the lamp.

## INTERFACE PIN CONNECTION

### (1) CN 3, 4(Backlight)

Backlight-side connector: BHSR-02VS-1(JST)

Inverter-side connector: SM02B-BHSS-1-TB

Pin No.	Symbol	Function
1, 2	CTH	VLH (High Voltage)

[Note] VBLH-VBLL = VL

### (2) CN 5, 6(Backlight)

Backlight-side connector: BHR-02VS-1(JST)

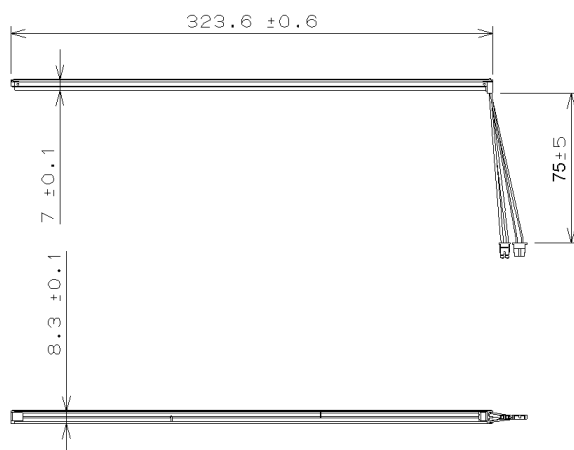
Inverter-side connector: SM02(4.0)B-BHS-1-TB

Pin No.	Symbol	Function
1, 2	CTL	VBLL (Low Voltage)

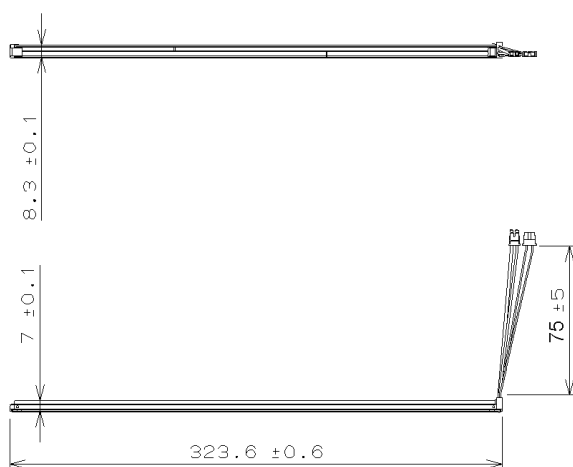
[Note] VBLH-VBLL = VL

## DRAWING OF OUTLINE DIMENTIONS

### (1) AA-L5902086G01 (Top)



### (2) AA-L5902087G01(Bottom)



## METHOD OF REPLACING THE LAMP UNIT

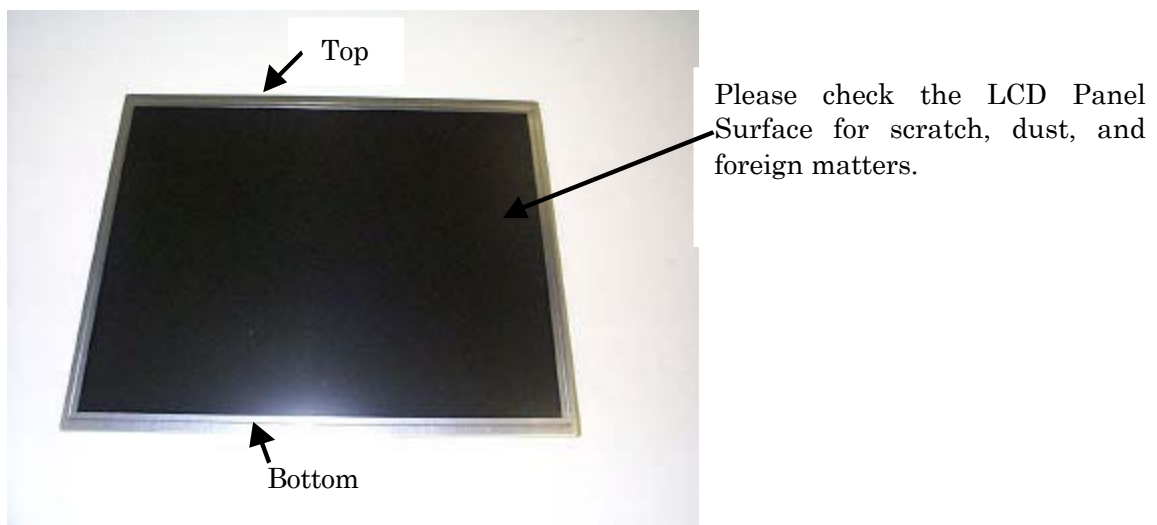
### (1) Precautions

Please pay attention to the following items while replacing the Lamp Unit.

- a. Please do not damage the LCD Panel Surface, and do not touch it with bare hands.  
(Wearing gloves is recommended.)
- b. Please be careful with electrostatics, and work in clean environment to prevent entering dust and/or foreign matters that will cause bad display image.  
(Using clean bench or similar environment is recommended.)
- c. Please be careful of the edge of the frame metal.
- d. Please replace top and bottom lamp units at the same time. Replace only one lamp unit will cause inferior display image.

### (2) Method of replacing the Lamp Unit

- 1) Put the TFT-LCD Module on the table.(LCD Panel Surface is upside.)



Picture 1

- 2) Turn the TFT-LCD Module upside down.

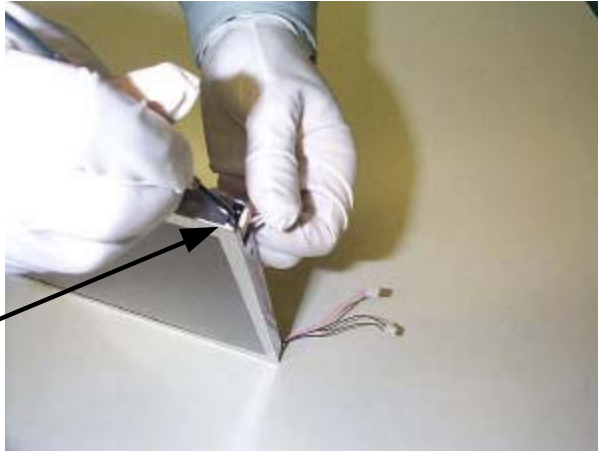
Please check the rear surface for dust and foreign matters.



Picture 2

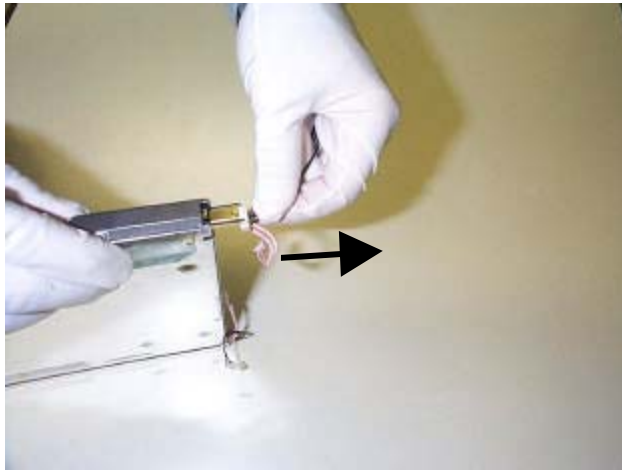
- 3) Stand the TFT-LCD Module up and push down the latch of rubber holder with that Lamp Unit fastens using a screw driver(-) and the like.

Push down the latch of rubber holder.



Picture 3

- 4) Pull the black cable slowly and remove the Lamp Unit. (Do not tug at the pink cable.)



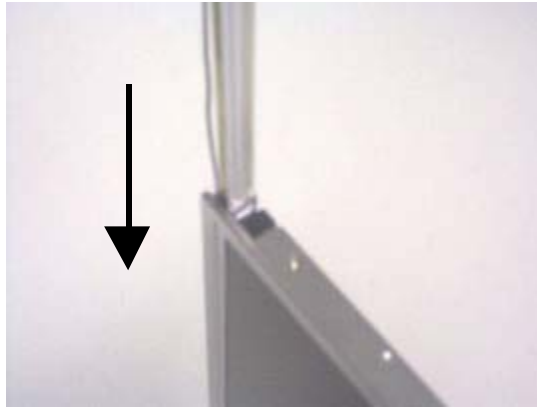
Picture 4

- 5) Remove the other Lamp Unit at the opposite(bottom) side of LCD Module in the same way. See.3) and 4)
- 6) Picture 5 shows the TFT-LCD Module after removing the Lamp Units.



Picture 5

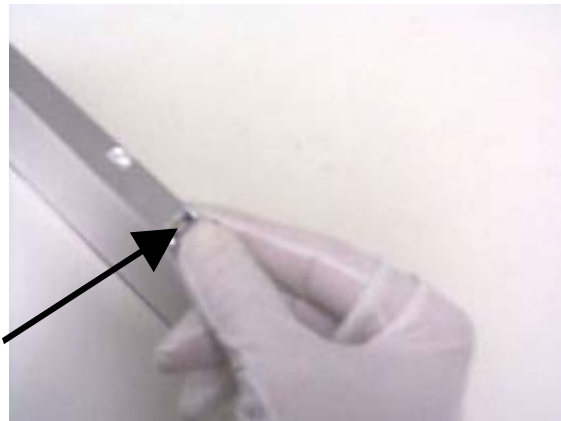
- 7) Prepare to insert the new Lamp Units.
- Open the package and take the new Lamp Units out.
  - Check the new Lamp Units for dust and foreign matters.
- 8) Stand the TFT-LCD module up and insert the new Lamp Unit.  
The light guide and reflector sheet should be inside of the Lamp Unit.  
Please be careful not to hurt your hands from the edge of the Lamp Unit.  
Please pay attention to insert direction.



Picture 6

- 9) Please insert Lamp Unit. After inserting the Lamp Unit, please check that the Lamp Unit is fastened with the latch of rubber holder.  
Please be careful not to tug at and bend the wire hard in handling.

Please check that the Lamp Unit is fastened with the latch of rubber holder.



Picture 7

- 10) Put the lamp cables in the trench of the plastic frame to keep inside of the module.



Picture 8

- 11) Insert the other Lamp Unit to the opposite(bottom) side of the LCD module in the same way.  
(See. 8) to 10)
- 12) After replacing the Lamp Units, please check the following items.
- Appearance of TFT-LCD Module is not changed after replacing Lamp Units.  
(See. Picture 1 and Picture 2)
  - There is no damage, dust, or foreign matters on the LCD Panel Surface.
  - Install the TFT-LCD Module then check turning on the lamps.



## **SPWG Notebook Panel Specification Version 3.5**

### **Purpose:**

SPWG (Standard Panel Working Group) was formed to establish a set of standard LCD panels with dimensions and interface characteristics that allow both notebook and LCD supplier industries to manage the volatile LCD supply and demand in an easier fashion. This effort enables panels from multiple LCD suppliers to be used in most notebooks (or other products utilizing these standard panels) that are designed around these Standard Panels without changing either the notebook/product or the LCD panel module tooling.

### **Summary:**

To date, the notebook and panel industry has been plagued by an overabundance of unique/custom designs from the many LCD suppliers in the industry. This has in turn, forced the notebook OEM's and other end-product users to change their packaging, interface design and tooling literally every time a new panel supplier or module has been used. This leads to schedule slippages, missed market opportunities, and logistic and product obsolescence problems. Similarly, many times this problem has blocked some LCD manufacturers from being considered as a potential supplier due to the magnitude of changes that their design would force on the notebook end product. As more panel suppliers come on line in the near future, this style of independent designs would only increase this problem for both the notebook OEM's as well as the LCD suppliers. In an attempt to lessen this problem, these requirements are being established with the aid of PC makers, notebook OEMs, LCD panel suppliers, and other parties related to the development of notebook displays.

Version 3.5 adds a new panel size 14.1"W and incorporates its option for an integrated inverter. Backward compatibility with existing SPWG panels is maintained. As in earlier versions no limits are placed on the LCD panel feature sets. A typo found in the 3.0 version of the 14.1" was also corrected. The JST connector part number was updated on all drawings. The Panel Power Sequence, section 5.9, was modified so that the "T" value definitions matched those of versions 1.0 and 2.0 of the SPWG spec.

### **Warranty:**

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**Support:**

The Standard Panel Working Group, which consists of many of the major notebook suppliers, in conjunction with many of the leading LCD suppliers, and other parties related to the development of notebook displays, have established these mechanical and electrical standards defined herein. This document has been refined through a number of proposal/feedback review cycles with these suppliers.

This document is intended as a reference document only for both notebook OEMs and panel suppliers and other parties related to the development of notebook displays. Users of this document should not base final end-product designs (notebook or other) on this document, but instead should utilize the display supplier's detailed drawings and specifications for full documentation.



### What is New in SPWG Version 3.5

<b>Item Description</b>	<b>SPWG Ver. 3.0</b>	<b>SPWG Ver. 3.5</b>
14.1" Panel dimension from datum line to top of panel.	Section 4.4 15.5mm+0.0,-2.5	Section 4.4 15.3mm+0.0,-2.5
14.1"W Panel defined	N/A	Section 4.5.
14.1"W Panel with Inverter defined	N/A	Section 8.5.
JAE Inverter I/O Connector introduced on 14.1"W panel with inverter drawing.	N/A	Section 8.5.
14.1"W JAE Inverter I/O Connector pin-out defined.	N/A	Section 8.1.2.
JST CCFL connector (N) suffix added to denote lead free version.	N/A	All panel drawings and Section 8.1.1.
Panel Power Sequence "T" value definitions were changed to be consistent with those SPWG version 2.0	Section 5.9.	Section 5.9.
14.1"W Inverter, PWM input voltage brightness control pin.	N/A	Section 8.1.2. pin 11

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- 4.0 Mechanical Properties:**
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- 6.0 Optical Measurement:**
- 7.0 Power Measurement:**
- 8.0 Inverter Integration:**
- 9.0 Screen Cosmetic Evaluation:**
- 10.0 Panel Reliability:**

## **1.0 Introduction and Overview:**

This document defines selected electrical interface requirements and mechanical dimensions for a series of industry compatible panels for XGA (1024x768), WXGA (1280x800, 1440x900), SXGA+ (1400x1050), WSXGA+ (1680x1050), UXGA (1600x1200), WUXGA (1920x1200), and QXGA (2048x1536) resolution LCD panels. These standard panels are defined as having 12.1"12.1"W, 13.3", 14.1", 14.1"W, 15.0", 15.4"W, and 17.0"W display screens. Through the DDC/EEDID interface, graphics controller BIOS and driver support is provided as well as support for Microsoft PC99 and future PCxxxx requirements.

With most panels used in portable computer designs today, the notebook OEM may have different interface cables, plastic or magnesium enclosures, bezels, bracket assemblies, and EMI shields for every panel used. For each of these parts, there are associated tooling changes required and schedule impacts relative to these tooling changes, to support the use of the different panels. Additionally, the associated documentation and logistics impacts for these different configurations are staggering. Many times these changes and schedule impacts, caused by these changes, eliminate many panel suppliers from being considered as potential 2<sup>nd</sup> sources.

This document establishes common panels for the multiple display sizes/aspect ratios. This enables a Standard Panel to be mounted in any system that has been designed to accept the maximum size Standard Panel of any size defined. The Standard Panel design has been developed to allow LCD panel suppliers the opportunity for product differentiation and still meet the intent of transparent usage across different platforms.

LCD manufacturers that have endorsed the SPWG standard include: AU Optronics, BOE/Hydis, Chi Mei, CPT, HannStar, Hitachi, IDTech, InnoLux, LG.Philips LCD, Mitsubishi, Quanta Display, Samsung, Sharp, Toppoly, Tottori Sanyo, and TMDisplay

Additionally, with the various requirements of PC00 and future PCxxxx versions, the incorporation of EEDID information will allow transparent usage with minimum changes to system BIOS or drivers. The end objective is to specify the panel-timing requirement so that no BIOS or driver changes are required with the use of a new panel

## **2.0 Reference Documents:**

The following documents form a part of this specification to the extent specified herein. The user of this document is advised to ensure they have the latest versions of these reference standards and documents.

- VESA Display Data Channel Standard, DDC2B
- VESA Enhanced Extended Display Identification Data
- VESA Flat Panel Display Measurement Standard, version 2.0
- Philips I<sup>2</sup>C Bus Specification – Data Handbook I<sup>2</sup>C Peripherals for Microcontrollers
- TIA/EIA-644 Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits

- Intel Common Panel Interface Specification, Nov. 2002, version 1.5.
- VESA file at [www.vesa.org](http://www.vesa.org) , FPDMSU.ppt
- VESA Coordinated Video Timing Generator, revision 1.1, April 9, 2003

### 3.0 **Panel Sizes, Resolutions, & Aspect Ratio:**

The notebook display panel sizes, resolutions, aspect ratios, pixel pitch, and pixels per inch covered by this specification are shown in the charts below.

Panel Size	Resolution	Pixels	Aspect Ratio
12.1", 13.3", 14.1", 15.0"	XGA	1024 x 768	4:3
12.1", 13.3", 14.1", 15.0"	SXGA+	1400 x 1050	4:3
14.1", 15.0"	UXGA	1600 x 1200	4:3
12.1"W, 14.1"W, 15.4"W, 17.0"W	WXGA	1280 x 800 1440 x 900	16:10
12.1"W, 14.1"W, 15.4"W, 17.0"W	WSXGA+	1680 x 1050	16:10
14.1"W, 15.4"W, 17.0"W	WUXGA	1920 x 1200	16:10
15.0"	QXGA	2048 x 1536	4:3

Panel Size	Resolution	Pixels	Aspect Ratio	Pixel Pitch	Pixels/Inch*
12.1"	XGA	1024 x 768	4:3	0.240	106
12.1"	SXGA+	1400 x 1050	4:3	0.176	144
12.1"W	WXGA	1280 x 800 1440 x 900	16:10	0.204 0.181	125 140
12.1"W	WSXGA+	1680 x 1050	16:10	0.155	164
13.3"	XGA	1024 x 768	4:3	0.264	96
13.3"	SXGA+	1400 x 1050	4:3	0.193	132
14.1"	XGA	1024 x 768	4:3	0.279	91
14.1"	SXGA+	1400 x 1050	4:3	0.204	125
14.1"	UXGA	1600 x 1200	4:3	0.179	142
14.1"W	WXGA	1280 x 800 1440 x 900	16:10	0.237 0.210	107 121
14.1"W	WSXGA+	1680 x 1050	16:10	0.180	141
14.1"W	WUXGA	1920 x 1200	16:10	0.158	161
15.0"	XGA	1024 x 768	4:3	0.296	86
15.0"	SXGA+	1400 x 1050	4:3	0.217	117
15.0"	UXGA	1600 x 1200	4:3	0.190	134
15.0"	QXGA	2048 x 1536	4:3	0.148	172
15.4"W	WXGA	1280 x 800 1440 x 900	16:10	0.259 0.230	98 110
15.4"W	WSXGA+	1680 x 1050	16:10	0.197	129
15.4"W	WUXGA	1920 x 1200	16:10	0.173	147
17.0"W	WXGA	1280 x 800 1440 x 900	16:10	0.287 0.255	89 100
17.0"W	WSXGA+	1680 x 1050	16:10	0.219	116
17.0"W	WUXGA	1920 x 1200	16:10	0.191	133

Approx values which may vary slightly by LCD supplier.

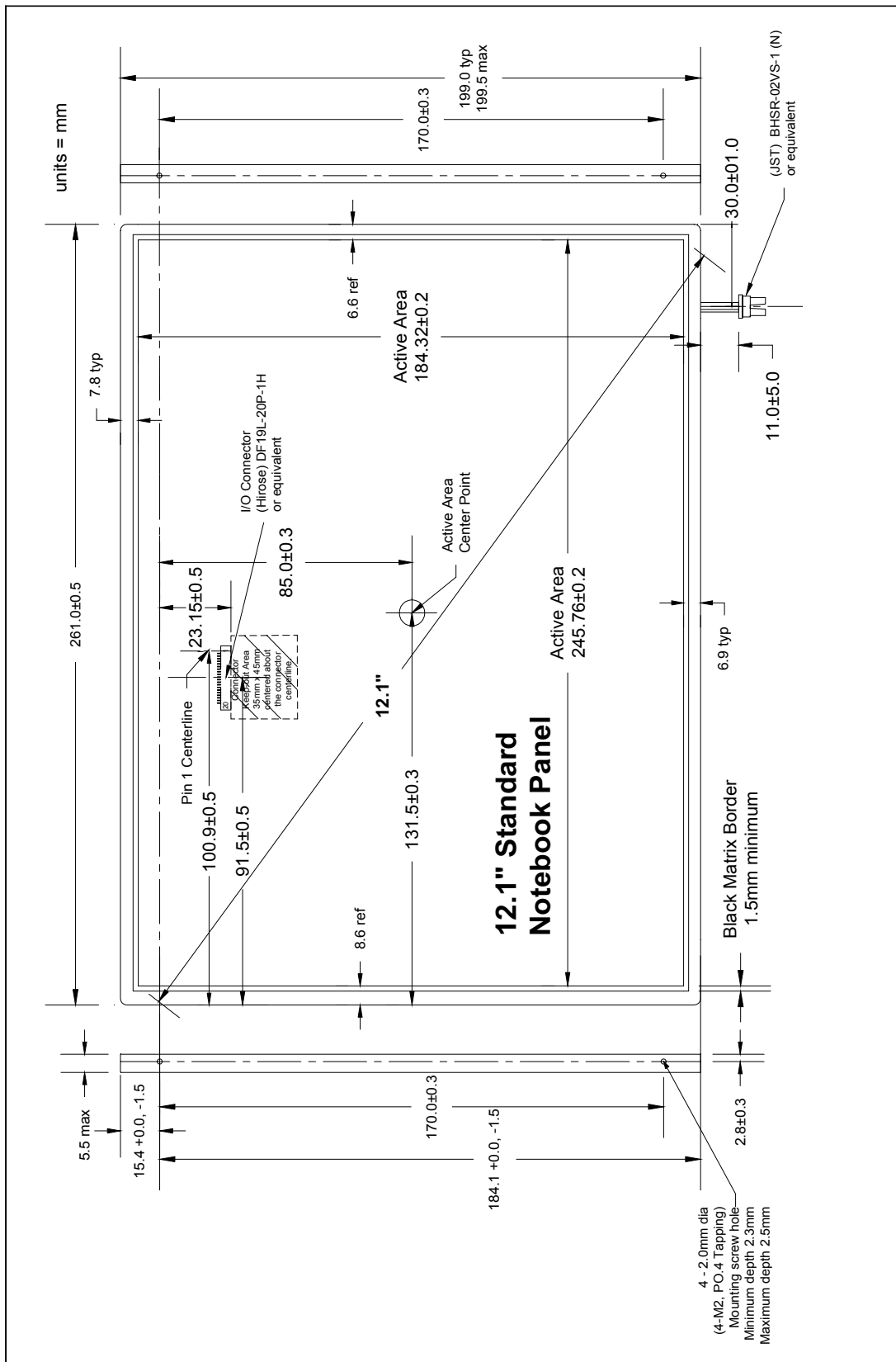
#### 4.0 **Mechanical Properties:**

Drawings for 12.1", 12.1W, 13.3", 14.1", 14.1"W, 15.0", 15.4"W, and 17.0"W display panels are included in this section.

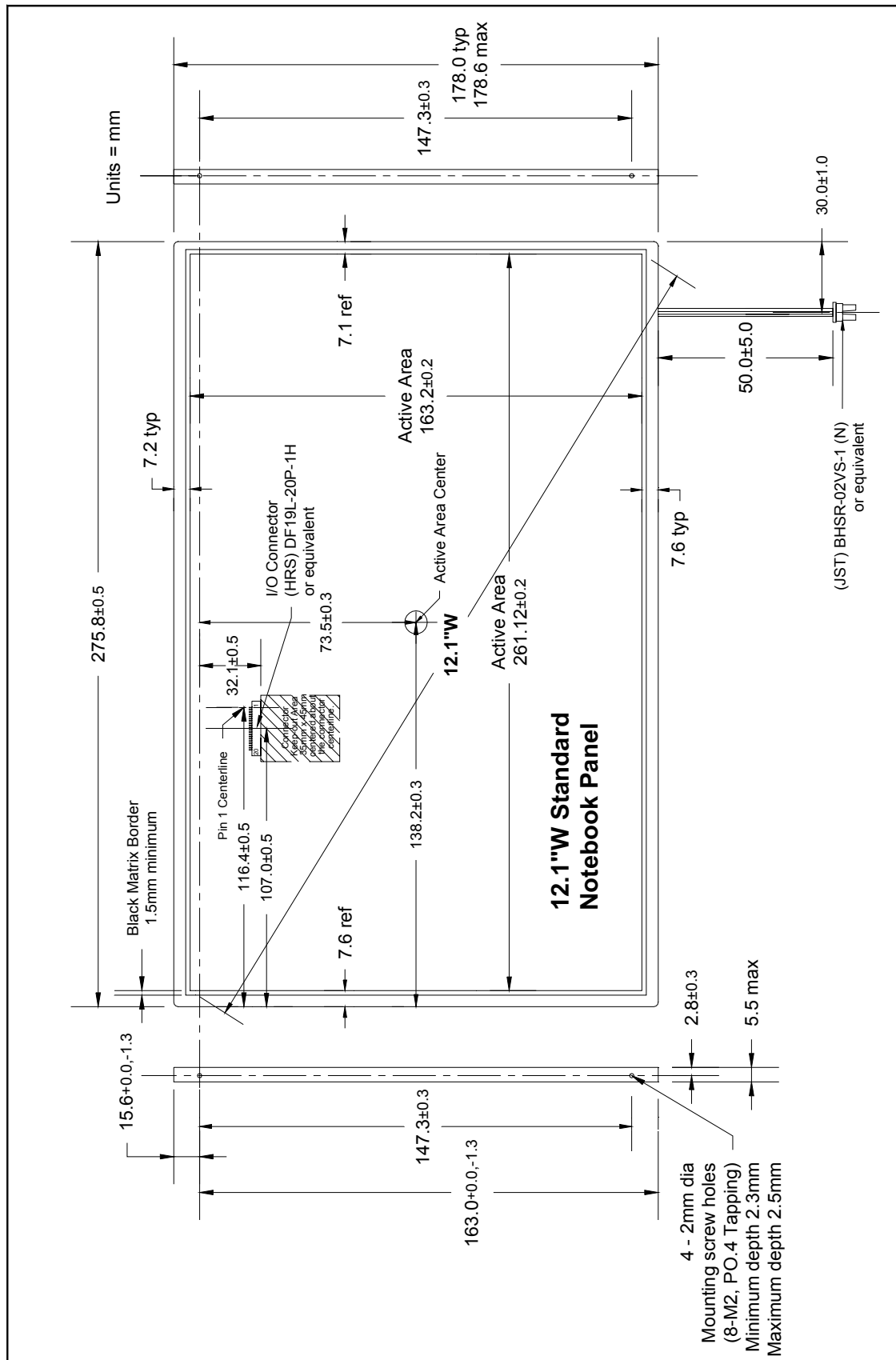
Notes:

1. Some changes have been made to the existing SPWG, version 2.0, drawings for the 13.3", 14.1", and 15.0" style B panels, to expand the LCD supplier base and make inverter integration easier. These changes are minor and should have minimal impact on backwards compatibility of existing panels. Changes include CCFL wire length updates to eliminate inverter pigtails and a change in the mounting hole depth to 2.3mm minimum, 2.5 maximum, which allows all LCD suppliers to participate. No minimum dimension was previously specified.
2. Notebook display panels have similar mechanical dimensions regardless of their screen resolution. There may, however, be a small variation in active area from one resolution to another caused by variations in pattern stepping capability during TFT fabrication. These small variations will not impact the active area center or the dimension of the system cover bezel.
3. The "units" for all drawings are millimeters.
4. The first and last pin numbers are labeled on the I/O connector.
5. The I/O connector is located on the rear of the panel and is shown as viewed from the panel's front surface.
6. The 30-pin I/O connector is listed as a JAE FI-Xx30Sx-HFxx or equivalent (locking design preferred). Connector manufacturers that have endorsed the SPWG standard include: DDK, FCI, Hirose, I-PEX, JAE, JST, KEL, LG Cable, Starconn, STM, Sunridge, and Uju.
7. The 20-pin I/O connector is listed as a HRS DF19L-20P-1H or equivalent. Connector manufacturers that have endorsed the SPWG standard include: DDK, FCI, Hirose, I-PEX, JAE, JST, KEL, LG Cable, Starconn, STM, Sunridge, and Uju.
8. Locking I/O connectors are backwards compatible with non-locking system cables.
9. These drawings cover the display panel module only and do not include an integrated inverter. If an inverter is added to the module the display panel's basic mechanical properties do not change.
10. To support the development of both newer display technologies and ultra thin panels, display panels that are too thin to reliably utilize mounting screws may be developed without incorporating the mounting holes. For these applications, the upper left mounting hole should be replaced with a  $0.5 \pm 0.1$ mm diameter reference locator hole,  $2.0 \pm 0.3$ mm from the face of the panel. Panel dimensioning should be referenced from the center of this location hole. As such this reference locating hole center becomes the 0, 0 point for dimensioning the panel

## 4.1 12.1" Standard Notebook Panel:



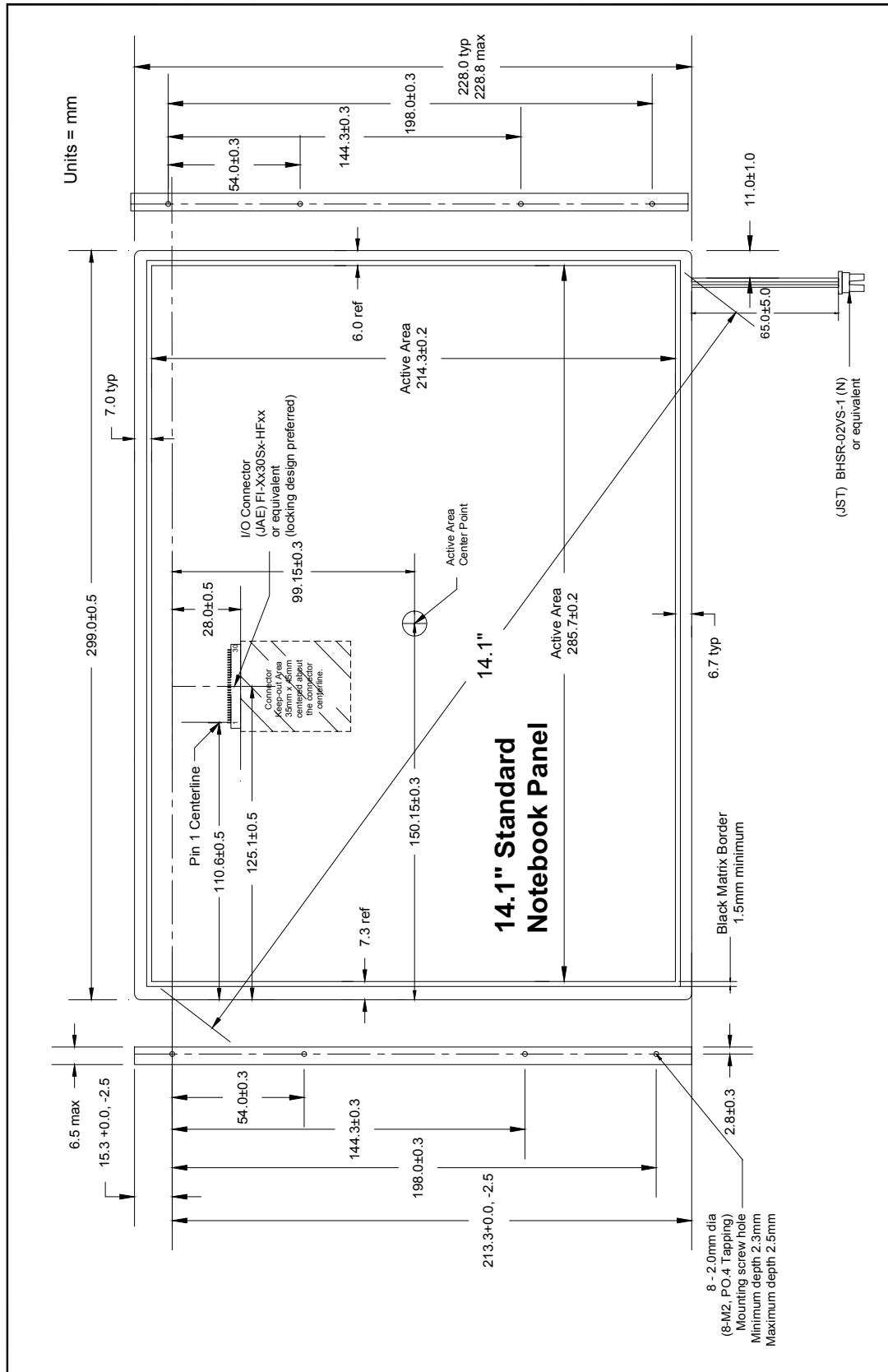
## 4.2 12.1"W Standard Notebook Panel





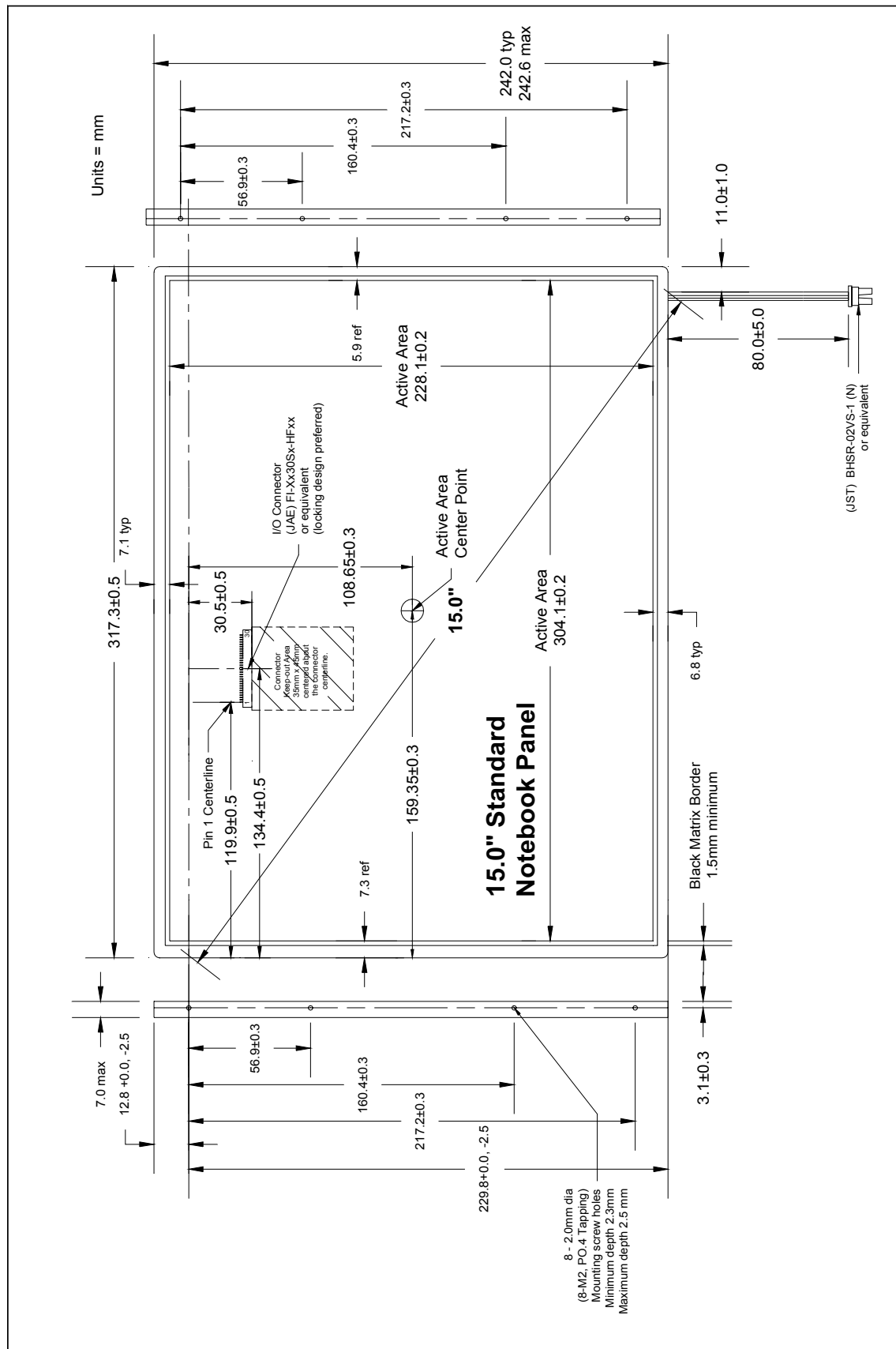


## 4.4 14.1" Standard Notebook Panel

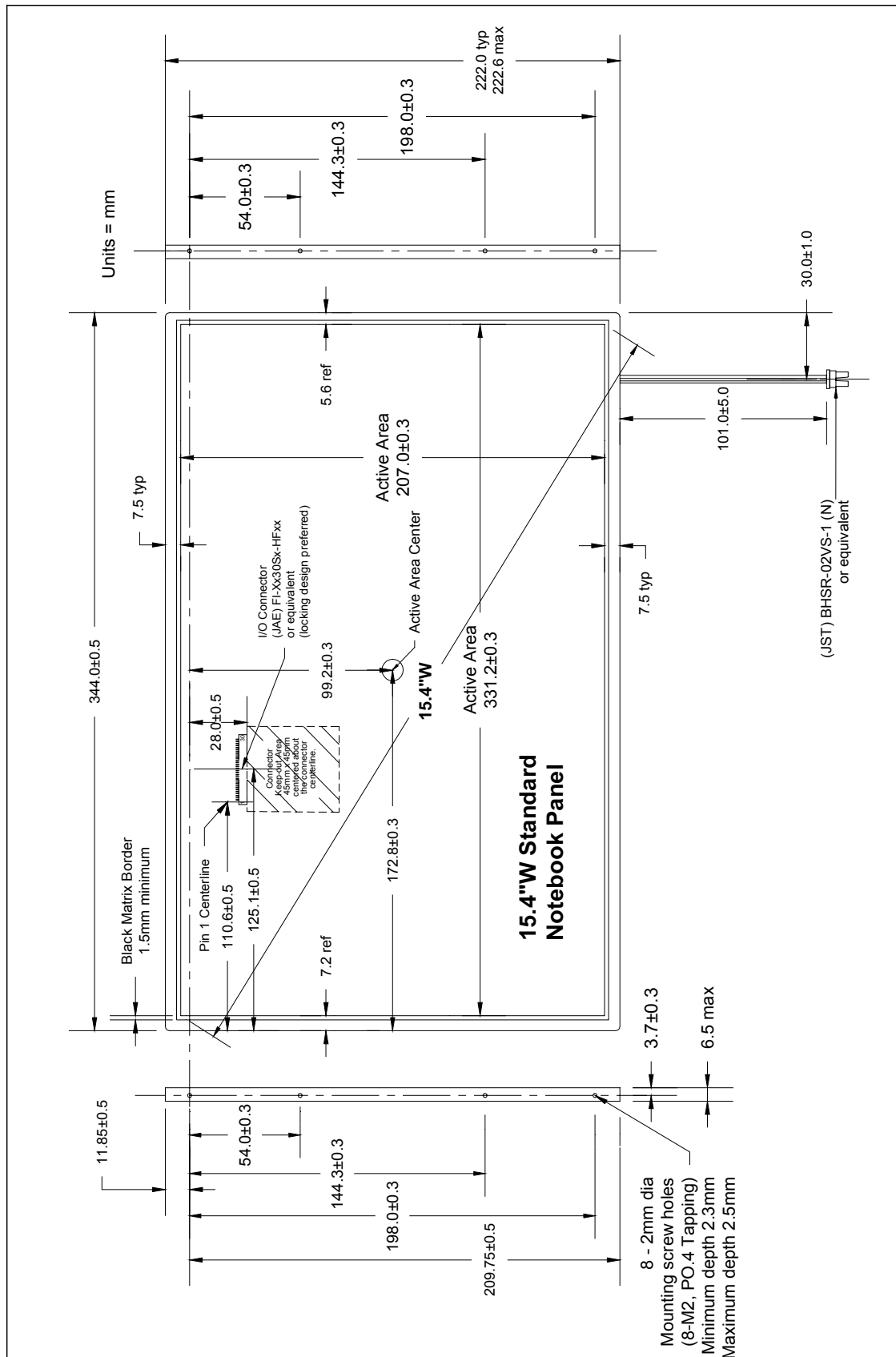




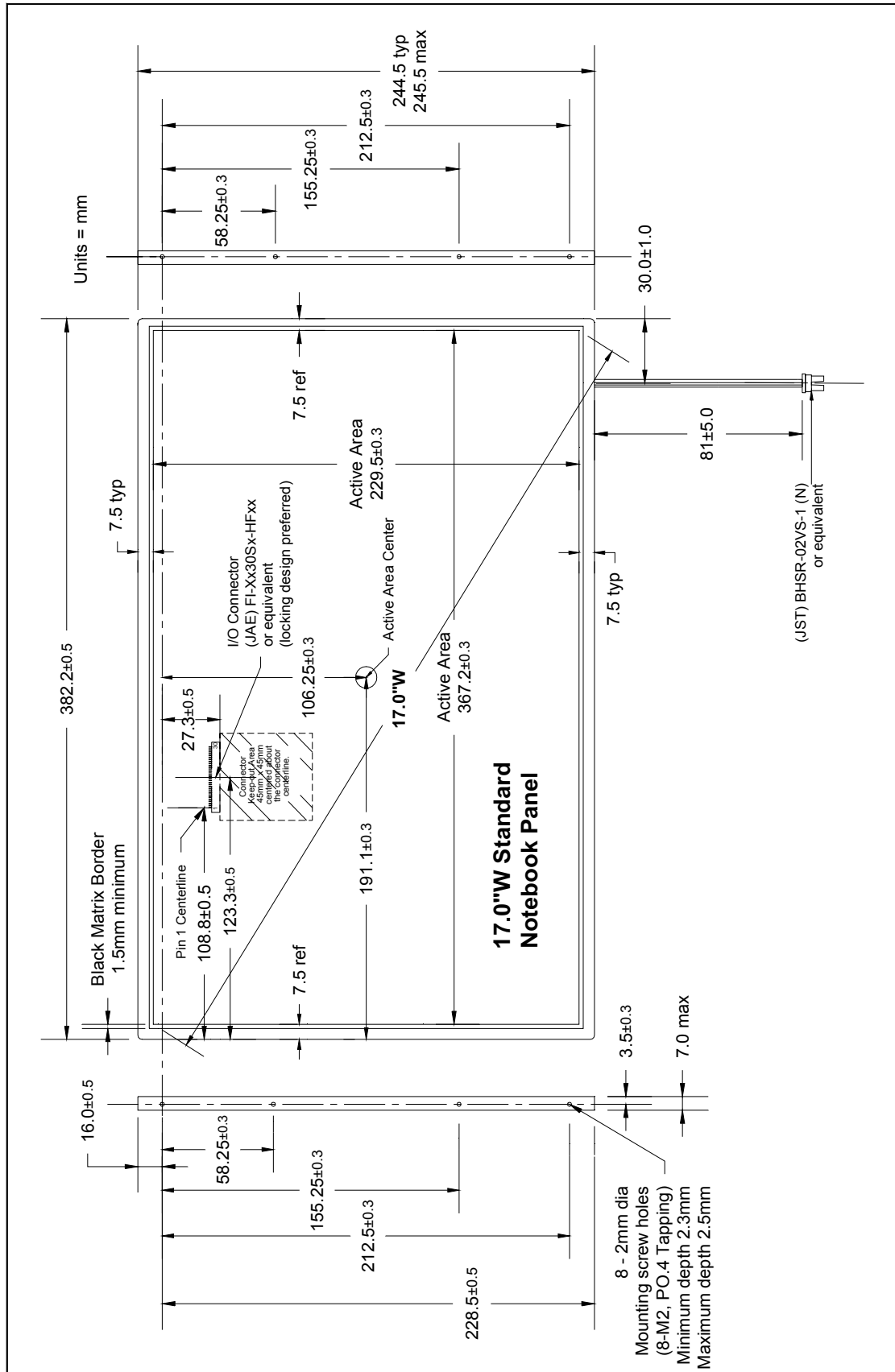
## 4.6 15.0" Standard Notebook Panel



## 4.7 15.4"W Standard Notebook Panel



## 4.8 17.0"W Standard Notebook Panel



## 5.0 Electrical Interface:

### 5.1 Connectors & Pin-Outs

#### 12.1" & 12.1"W Display Interface Cable Pin Assignments

I/O Connector: (HRS) DF19L-20P-1H or equivalent (1 Channel LVDS)

Pin	Symbol	Pin Function
1	VSS	Ground
2	VDD	Power Supply, 3.3 V (typical)
3	VDD	Power Supply, 3.3 V (typical)
4	V <sub>EEDID</sub>	DDC 3.3 V power
5	Tp	Reserved for LCD supplier test point
6	Clk <sub>EEDID</sub>	DDC Clock
7	Data <sub>EEDID</sub>	DDC Data
8	Odd R <sub>IN</sub> 0 -	- LVDS differential data input, R0 – R5, G0
9	Odd R <sub>IN</sub> 0 +	+ LVDS differential data input, R0 – R5, G0
10	VSS	Ground
11	Odd R <sub>IN</sub> 1 -	- LVDS differential data input, G1 – G5, B0 – B1
12	Odd R <sub>IN</sub> 1 +	+ LVDS differential data input, G1 – G5, B0 – B1
13	VSS	Ground
14	Odd R <sub>IN</sub> 2 -	- LVDS differential data input, B2 – B5, HS/VS/DE
15	Odd R <sub>IN</sub> 2 +	+ LVDS differential data input, B2 – B5, HS/VS/DE
16	VSS	Ground
17	Odd Clk <sub>IN</sub> -	- LVDS differential clock input
18	Odd Clk <sub>IN</sub> +	+ LVDS differential clock input
19	VSS	Ground
20	VSS	Ground

#### 13.3", 14.1", 14.1"W, 15.0", 15.4"W, and 17.0"W Display Interface Cable Pin Assignments

I/O Connector: (JAE) FI-Xx30Sx-HFxx or equivalent (2 Channel LVDS)

Pin	Symbol	Pin Function
1	VSS	Ground
2	VDD	Power Supply, 3.3 V (typical)
3	VDD	Power Supply, 3.3 V (typical)
4	V <sub>EEDID</sub>	DDC 3.3 V power
5	Tp	Reserved for LCD supplier test point
6	Clk <sub>EEDID</sub>	DDC Clock
7	Data <sub>EEDID</sub>	DDC Data
8	Odd R <sub>IN</sub> 0 -	- LVDS differential data input, R0 – R5, G0 (odd pixels on SXGA+ & higher resolutions)
9	Odd R <sub>IN</sub> 0 +	+ LVDS differential data input, R0 – R5, G0 (odd pixels on SXGA+ & higher resolutions)
10	VSS	Ground
11	Odd R <sub>IN</sub> 1 -	- LVDS differential data input, G1 – G5, B0 – B1 (odd pixels on SXGA+ & higher resolutions)
12	Odd R <sub>IN</sub> 1 +	+ LVDS differential data input, G1 – G5, B0 – B1 (odd pixels on SXGA+ & higher resolutions)
13	VSS	Ground
14	Odd R <sub>IN</sub> 2 -	- LVDS differential data input, B2 – B5, HS/VS/DE (odd pixels on SXGA+ & higher resolutions)
15	Odd R <sub>IN</sub> 2 +	+ LVDS differential data input, B2 – B5, HS/VS/DE (odd pixels on SXGA+ & higher resolutions)
16	VSS	Ground
17	Odd Clk <sub>IN</sub> -	- LVDS differential clock input (odd pixels on SXGA+ & higher resolutions)
18	Odd Clk <sub>IN</sub> +	+ LVDS differential clock input (odd pixels on SXGA+ & higher resolutions)
19	VSS	Ground
20	Even R <sub>IN</sub> 0 -	- LVDS differential data input, even pixels, R0 – R5, G0 (NC on XGA resolution)
21	Even R <sub>IN</sub> 0 +	+ LVDS differential data input, even pixels, R0 – R5, G0 (NC on XGA resolution)
22	VSS	Ground
23	Even R <sub>IN</sub> 1 -	- LVDS differential data input, even pixels, G1 – G5, B0 – B1 (NC on XGA resolution)
24	Even R <sub>IN</sub> 1 +	+ LVDS differential data input, even pixels, G1 – G5, B0 – B1 (NC on XGA resolution)
25	VSS	Ground
26	Even R <sub>IN</sub> 2 -	- LVDS differential data input, even pixels, B2 – B5, HS/VS/DE (NC on XGA resolution)
27	Even R <sub>IN</sub> 2 +	+ LVDS differential data input, even pixels, B2 – B5, HS/VS/DE (NC on XGA resolution)
28	VSS	Ground
29	Even Clk <sub>IN</sub> -	- LVDS differential clock input, even pixels (NC on XGA resolution)
30	Even Clk <sub>IN</sub> +	+ LVDS differential clock input, even pixels (NC on XGA resolution)

## 5.2 Signal Timing

Notebook signal timing is 18 bit as defined VESA Coordinated Video Timing Generator, revision 1.1, April 9, 2003, with reduced blanking.

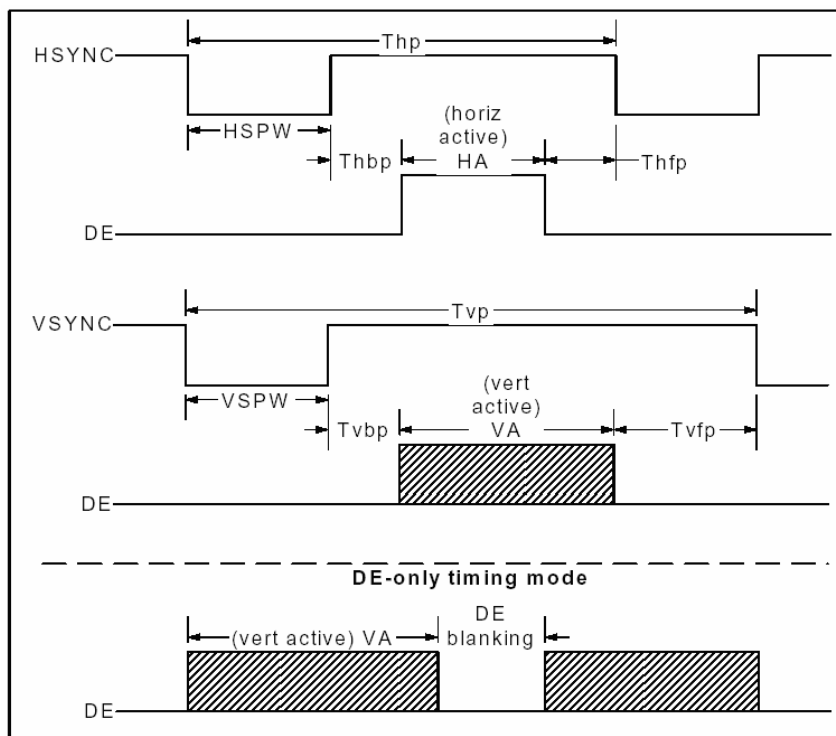
### Single LVDS Channel Primary Timing Values at a 60 Hz Frame Rate

Resolution		XGA	SXGA+	UXGA	WXGA(I)	WXGA(II)	WSXGA+	WUXGA	QXGA
		1024x768	1400x1050	1600x1200	1280x800	1440x900	1680x1050	1920x1200	2048x1536

Overall Dot Clock		Typ	Typ	Typ	Typ	Typ	Typ	Typ	Units	
FPD	Dot Clock Freq.	56.000	101.000	130.250	71.000	88.750	119.000	154.000	209.250	MHz
FPDP	Dot Clock Period	17.857	9.901	7.678	14.085	11.268	8.403	6.494	4.779	nsec
DCSS	Clock Spread	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	% of Dot

Horizontal Parameters		Typ	Typ	Typ	Typ	Typ	Typ	Typ	Units	
HA	Horizontal Active	1024	1400	1600	1280	1440	1680	1920	2048	Pixels
HFP	Horiz. Front Porch	48	48	48	48	48	48	48	48	Pixels
HSPW	Horiz. Sync PW	32	32	32	32	32	32	32	32	Pixels
HBP	Horiz. Back Porch	80	80	80	80	80	80	80	80	Pixels
HP	Horizontal Period	1184	1560	1760	1440	1600	1840	2080	2208	Pixels
HP	Horizontal Period	21.14	15.44	13.51	20.28	18.03	15.46	13.50	10.55	μsec
HF	Horizontal Freq.	47.30	64.74	74.01	49.31	55.47	64.67	74.04	94.77	KHz

Vertical Parameters		Typ	Typ	Typ	Typ	Typ	Typ	Typ	Units	
VA	Vertical Active	768	1050	1200	800	900	1050	1200	1536	Lines
VFP	Vertical Front Porch	3	3	3	3	3	3	3	3	Lines
VSPW	Vert. Sync PW	4	4	4	6	6	6	6	4	Lines
VBP	Vertical Bk Porch	15	23	28	14	17	21	26	37	Lines
VP	Vertical Period	790	1080	1235	823	926	1080	1235	1580	Lines
VFP	Vertical Frequency	59.87	59.95	59.92	59.91	59.90	59.98	59.95	59.98	Hz



### 5.3 Signal Timing Waveforms Parameters

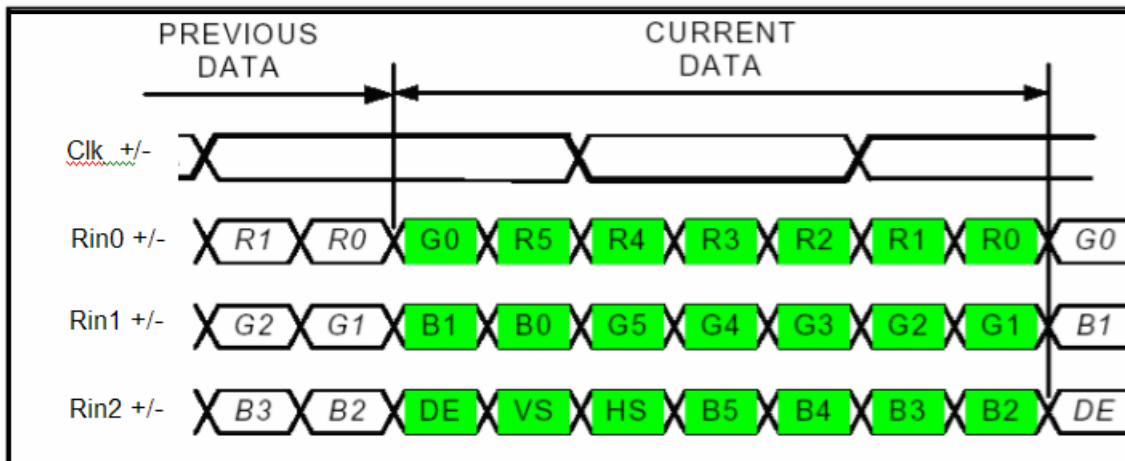
Name	Definition
Thp	The total horizontal line time from the start of one horizontal sync pulse to the start of the subsequent pulse. This time equals the sum of Thbp, HA, and Thfp. It is expressed in pixels.
HA	Horizontal Active. This is the time during which DE is at the active level. Active pixel data is transmitted during this time. It is expressed in pixels.
Thbp	Horizontal Back Porch time. This is the time from the end of the horizontal sync pulse to the start of the active pixel data stream (HA). It is expressed in pixels.
HSPW	Horizontal Sync Pulse Width. The time the horizontal sync pulse is active. It is expressed in pixels.
Thfp	Horizontal Front Porch time. This is the time between the end of the active pixel data stream (HA) to the start of the subsequent horizontal sync pulse. It is expressed in pixels.
Tvp	The total vertical frame time from the start of one vertical sync pulse to the start of the subsequent pulse. This time equals the sum of Tvbp, VA, and Tvfp. It is expressed in lines.
VA	Vertical Active. This is the time during which active pixel data is being transmitted for the frame. This is the time from the beginning of the horizontal sync pulse for the first active display line of the frame to the beginning of the horizontal sync pulse for the first line after the last active display line of the frame. An active display line is one in which DE is active. It is expressed in lines.
Tvbp	Vertical Back Porch time. This is the time from the end of the vertical sync pulse to the beginning of the horizontal sync pulse for the first active display line of the frame. An active display line is one in which DE is active. It is expressed in lines.
VSPW	Vertical Sync Pulse Width. The time the vertical sync pulse is active. It is expressed in lines.
Tvfp	Vertical Front Porch time. This is the time between the end of the horizontal sync pulse for the first line after the last active display line of the frame to the start of the subsequent vertical sync pulse. An active display line is one in which DE is active. It is expressed in lines.



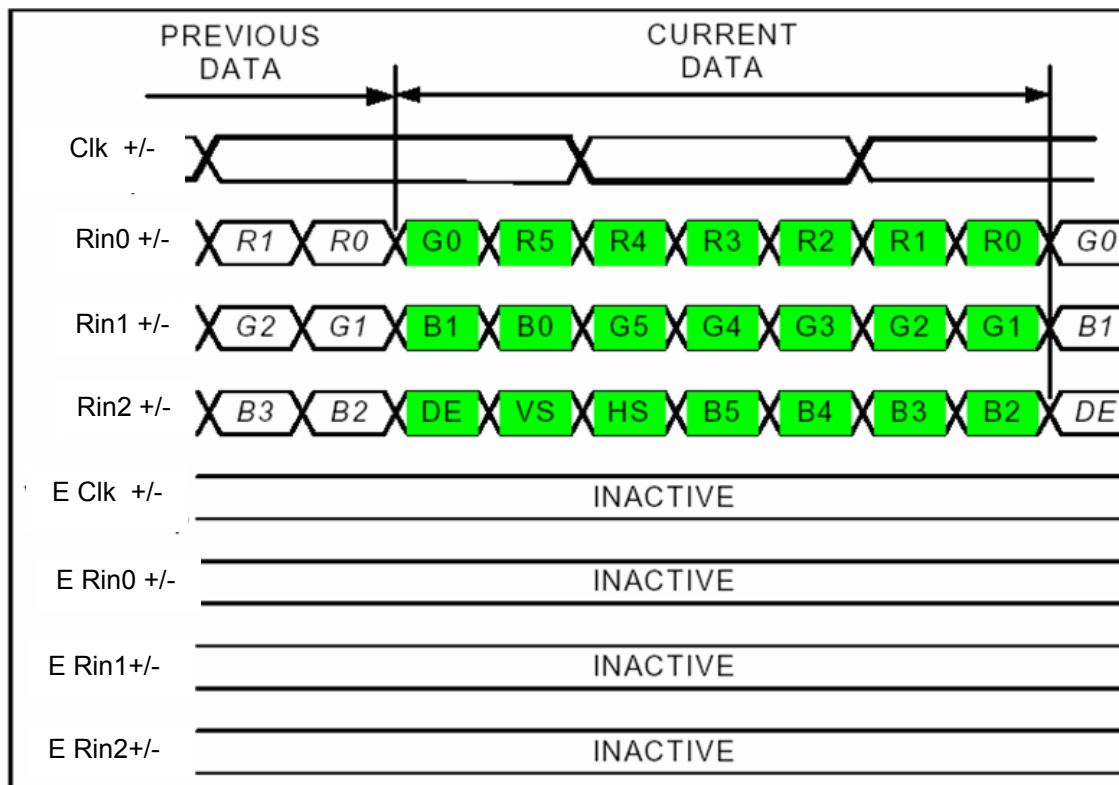
## 5.4 LVDS Data and Control Signal Interface

The panel LVDS signals interface should meet the requirements of TAI/EAI-644. The figures below show mapping diagrams of each LVDS channel. These diagrams define the current 6 bit, 18bpp, notebook panel LVDS addressing scheme.

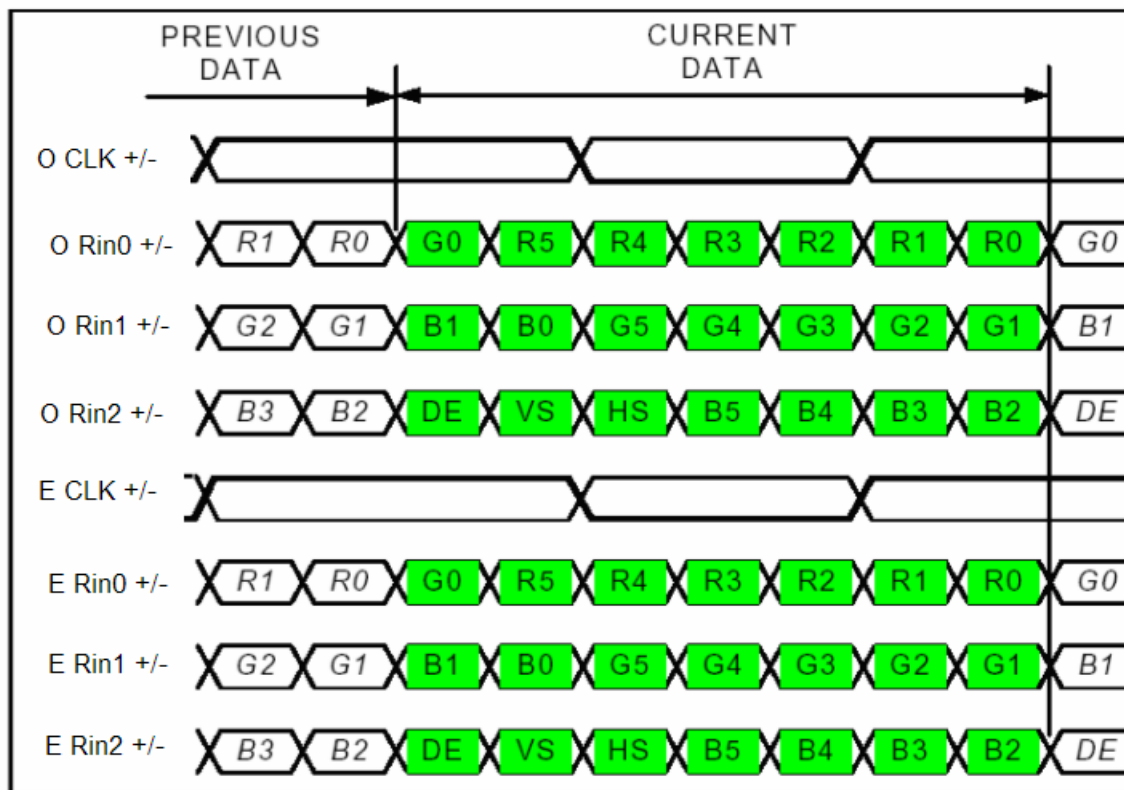
### Single Channel LVDS Data Mapping (18bpp) 20-Pin Connector



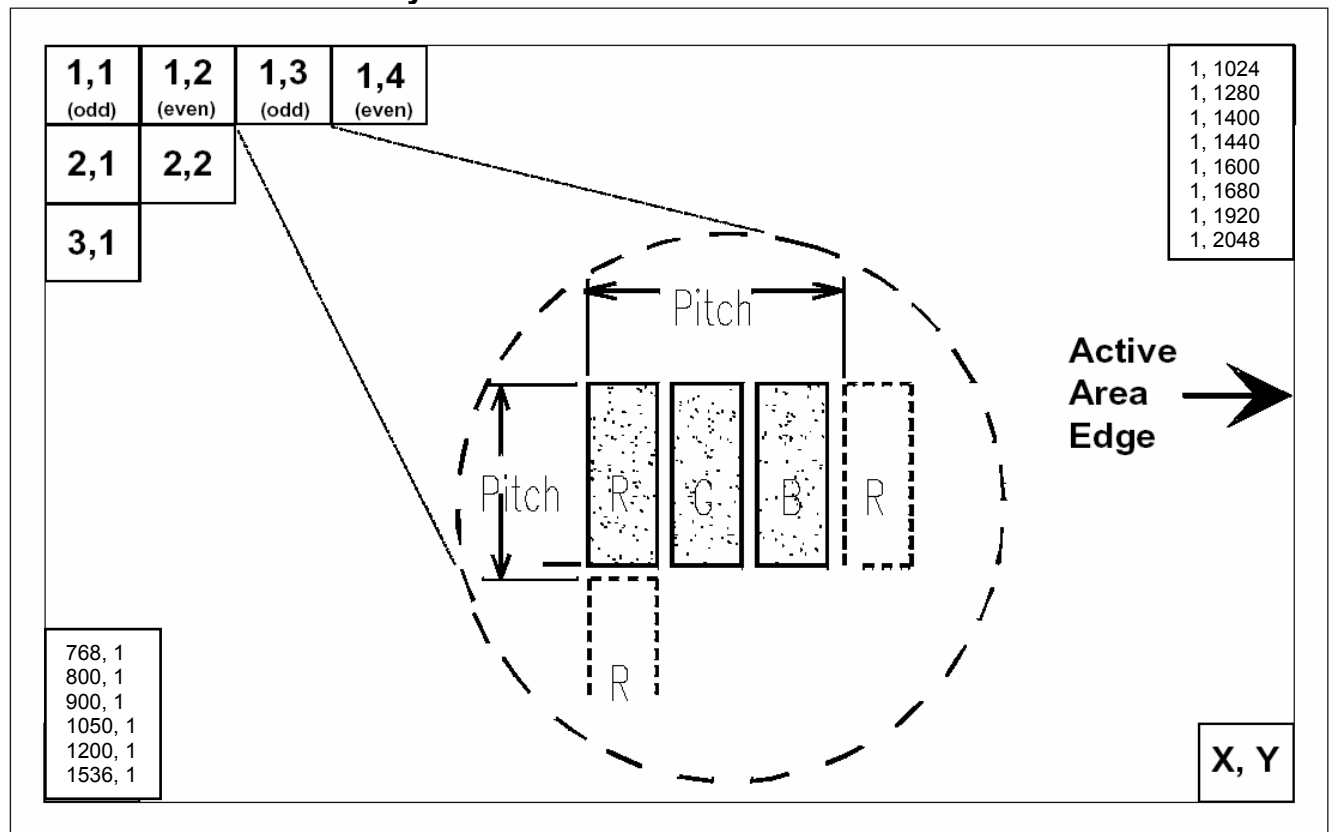
### 5.5 Single Channel LVDS Data Mapping (18bpp) 30-Pin Connector



## 5.6 Dual Channel LVDS Data Mapping (18bpp) 30-Pin Connector



## 5.7 Active Area Pixel Layout



- 5.8** This is the EDID (Enhanced Extended Display Identification Data) data format to support displays as defined in the VESA Plug & Display.

### Header

Byte (dec)	Byte (hex)	Field Name and Comments	Value (hex)	Value (binary)
0	00	Header	00	00000000
1	01	Header	FF	11111111
2	02	Header	FF	11111111
3	03	Header	FF	11111111
4	04	Header	FF	11111111
5	05	Header	FF	11111111
6	06	Header	FF	11111111
7	07	Header	00	00000000

### Vendor / Product ID / EDID Version

Byte (dec)	Byte (hex)	Field Name and Comments	Value (hex)	Value (binary)
8	08	EISA manufacture code = 3 Character ID		
9	09	EISA manufacture code (Compressed ASCII)		
10	0A	Panel Supplier Reserved – Product Code		
11	0B	Panel Supplier Reserved – Product Code		
12	0C	LCD module Serial No – Preferred but Optional (“0” if not used)	00	00000000
13	0D	LCD module Serial No – Preferred but Optional (“0” if not used)	00	00000000
14	0E	LCD module Serial No – Preferred but Optional (“0” if not used)	00	00000000
15	0F	LCD module Serial No – Preferred but Optional (“0” if not used)	00	00000000
16	10	Week of manufacture		
17	11	Year of manufacture		
18	12	EDID structure version # = 1 (EDID V1.3)	01	00000001
19	13	EDID revision # = 3 (Release A, Rev 1, 2/9/2000)	03	00000011

### Display Parameters

Byte (dec)	Byte (hex)	Field Name and Comments	Value (hex)	Value (binary)
20	14	Video I/P definition = Digital I/P (80h)	80	10000000
21	15	Max H image size = (Rounded to cm)		
22	16	Max V image size = (Rounded to cm)		
23	17	Display gamma = (gamma × 100) - 100 = Example: ( 2.2 × 100 ) – 100 = 120		
24	18	Feature support ( no DPMS, Active off, RGB, timing BLK 1)	0A	00001010

**Panel Color Coordinates**

Byte (dec)	Byte (hex)	Field Name and Comments	Value (hex)	Value (binary)
25	19	Red/Green Low bit (RxRy/GxGy)		
26	1A	Blue/White Low bit (BxBy/WxWy)		
27	1B	Red X Rx = 0.xxx		
28	1C	Red Y Ry = 0.xxx		
29	1D	Green X Gx = 0.xxx		
30	1E	Green Y Gy = 0.xxx		
31	1F	Blue X Bx = 0.xxx		
32	20	Blue Y By = 0.xxx		
33	21	White X Wx = 0.xxx		
34	22	White Y Wy = 0.xxx		

**Established Timings**

Byte (dec)	Byte (hex)	Field Name and Comments	Value (hex)	Value (binary)
35	23	Established timings 1 (00h if not used)	00	00000000
36	24	Established timings 2 (00h if not used)	00	00000000
37	25	Manufacturer's timings (00h if not used)	00	00000000

**Standard Timing ID**

Byte (dec)	Byte (hex)	Field Name and Comments	Value (hex)	Value (binary)
38	26	Standard timing ID1 (01h if not used)	01	00000001
39	27	Standard timing ID1 (01h if not used)	01	00000001
40	28	Standard timing ID2 (01h if not used)	01	00000001
41	29	Standard timing ID2 (01h if not used)	01	00000001
42	2A	Standard timing ID3 (01h if not used)	01	00000001
43	2B	Standard timing ID3 (01h if not used)	01	00000001
44	2C	Standard timing ID4 (01h if not used)	01	00000001
45	2D	Standard timing ID4 (01h if not used)	01	00000001
46	2E	Standard timing ID5 (01h if not used)	01	00000001
47	2F	Standard timing ID5 (01h if not used)	01	00000001
48	30	Standard timing ID6 (01h if not used)	01	00000001
49	31	Standard timing ID6 (01h if not used)	01	00000001
50	32	Standard timing ID7 (01h if not used)	01	00000001
51	33	Standard timing ID7 (01h if not used)	01	00000001
52	34	Standard timing ID8 (01h if not used)	01	00000001
53	35	Standard timing ID8 (01h if not used)	01	00000001

**Timing Descriptor #1**

Byte (dec)	Byte (hex)	Field Name and Comments	Value (hex)	Value (binary)
54	36	Pixel Clock/10,000 (LSB)		
55	37	Pixel Clock/10,000 (MSB)		
56	38	Horizontal Active = xxxx pixels (lower 8 bits) <b>Note 2</b>		
57	39	Horizontal Blanking (Thbp) = xxxx pixels (lower 8 bits)		
58	3A	Horizontal Active/Horizontal blanking (Thbp) (upper4:4 bits)		
59	3B	Vertical Active = xxxx lines		
60	3C	Vertical Blanking (Tvbp) = xxxx lines (DE Blanking typ. For DE only panels)		
61	3D	Vertical Active : Vertical Blanking (Tvbp) (upper4:4 bits)		
62	3E	Horizontal Sync, Offset (Thfp) = xxxx pixels		
63	3F	Horizontal Sync, Pulse Width = xxxx pixels		
64	40	Vertical Sync, Offset (Tvfp) = xx lines Sync Width = xx lines		
65	41	Horizontal Vertical Sync Offset/Width upper 2 bits		
66	42	Horizontal Image Size =xxx mm		
67	43	Vertical image Size = xxx mm		
68	44	Horizontal Image Size / Vertical image size		
69	45	Horizontal Border = 0 (Zero for Notebook LCD)	00	00000000
70	46	Vertical Border = 0 (Zero for Notebook LCD)	00	00000000
71	47	Non-interlaced, Normal, no stereo, Separate sync, H/V pol Negatives, <b>DE only note: LSB is set to "1" if panel is DE-timing only. H/V can be ignored.</b>	18 (19)	00011000 00011001

**Timing Descriptor #2 Alternative Panel Timing**

Byte (dec)	Byte (hex)	Field Name and Comments	Value (hex)	Value (binary)
72	48	Pixel Clock/10,000 (LSB)		
73	49	Pixel Clock/10,000 (MSB)		
74	4A	Horizontal Active = xxxx pixels (lower 8 bits) <b>Note 2</b>		
75	4B	Horizontal Blanking (Thbp) = xxxx pixels (lower 8 bits)		
76	4C	Horizontal Active/Horizontal blanking (Thbp) (upper4:4 bits)		
77	4D	Vertical Active = xxxx lines		
78	4E	Vertical Blanking (Tvbp) = xxxx lines (DE Blanking typ. For DE only panels)		
79	4F	Vertical Active : Vertical Blanking (Tvbp) (upper4:4 bits)		
80	50	Horizontal Sync, Offset (Thfp) = xxxx pixels		
81	51	Horizontal Sync, Pulse Width = xxxx pixels		
82	52	Vertical Sync, Offset (Tvfp) = xx lines Sync Width = xx lines		
83	53	Horizontal Vertical Sync Offset/Width upper 2 bits		
84	54	Horizontal Image Size =xxx mm		
85	55	Vertical image Size = xxx mm		
86	56	Horizontal Image Size / Vertical image size		
87	57	Horizontal Border = 0 (Zero for Notebook LCD)	00	00000000
88	58	Vertical Border = 0 (Zero for Notebook LCD)	00	00000000
89	59	Module "A" Revision = Example: 00, 01, 02, 03, etc.		

**Timing Descriptor #3**

Byte (dec)	Byte (hex)	Field Name and Comments	Value (hex)	Value (binary)
90	5A	Flag	00	00000000
91	5B	Flag	00	00000000
92	5C	Flag	00	00000000
93	5D	Dummy Descriptor	FE	11111110
94	5E	Flag	00	00000000
95	5F	PC Maker P/N 1 <sup>st</sup> Character		
96	60	PC maker P/N 2 <sup>nd</sup> Character		
97	61	PC maker P/N 3 <sup>rd</sup> Character		
98	62	PC maker P/N 4 <sup>th</sup> Character		
99	63	PC maker P/N 5 <sup>th</sup> Character		
100	64	LCD Supplier EEDID Revision #		
101	65	Manufacturer P/N		
102	66	Manufacturer P/N		
103	67	Manufacturer P/N		
104	68	Manufacturer P/N		
105	69	Manufacturer P/N		
106	6A	Manufacturer P/N		
107	6B	Manufacturer P/N (If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)		

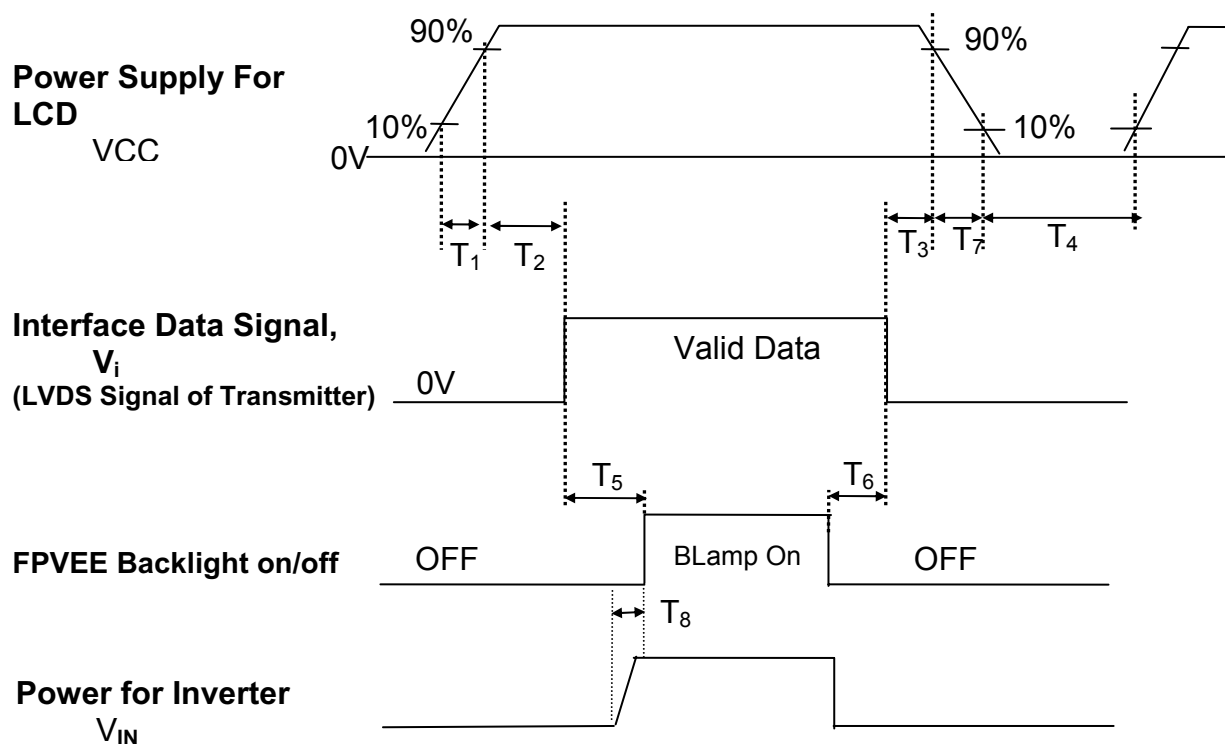
**Timing Descriptor #4**

Byte (dec)	Byte (hex)	Field Name and Comments	Value (hex)	Value (binary)
108	6C	Flag	00	00000000
109	6D	Flag	00	00000000
110	6E	Flag	00	00000000
111	6F	Data Type Tag:	FE	11111110
112	70	Flag	00	00000000
113	71	SMBUS Value = XX nits		Value
114	72	SMBUS Value = XX nits		Value
115	73	SMBUS Value = XX nits		Value
116	74	SMBUS Value = XX nits		Value
117	75	SMBUS Value = XX nits		Value
118	76	SMBUS Value = XXX nits		Value
119	77	SMBUS Value = XXX nits		Value
120	78	SMBUS Value = max nits (Typically = 00h, XXX nits)		Value
121	79	Number of LVDS channels = 1 or 2		
122	7A	Panel Self Test (00 – Not Present, 01 – Present)		00000000
123	7B	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	0A	00001010
124	7C	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000
125	7D	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000

Byte (dec)	Byte (hex)	Field Name and Comments	Value (hex)	Value (binary)
126	7E	Extension flag (# of optional 128 EDID extension blocks to follow, Typ = 0)	00	00000000
127	7F	Checksum (The 1-byte sum of all 128 bytes in this EDID block shall = 0)		

**EEDID Notes:**

1. See page 16 for “Timing Waveform Parameters” definitions.
2. Horizontal Active (HA), byte 38h, is true active pixels.  $HA_{\text{pixel clk}}$  value, bytes 55 & 56, is HA for XGA and HA/2 for WSXGA+ and above resolutions.
3. Timing Descriptor #2 may be used for timings other than 60Hz

**5.9 Panel Power Sequence****Power Sequence Timing**

Parameter	Value			Units
	Min.	Typ.	Max.	
T1	0.5	-	10	(ms)
T2	0	-	50	(ms)
T3	0	-	50	(ms)
T4	200	-	-	(ms)
T5	200	-	-	(ms)
T6	200	-	-	(ms)
T7	0	-	10	(ms)
T8	10	-	-	(ms)

## 5.10 Panel Backlight Interface

The panel CCFL cable should be terminated with a JST BHSR-02VS-1 connector, or equivalent. The lamp wires exiting the panel should be sufficiently protected so that normal movement of these wires during cover assembly will not cause them to be damaged.

### Backlight Electrical Interface

Pin No.	Signal	Level	Function
1	$V_{CCFL}$	AC	Power supply for CCFL
2	Gnd Return	~GND	Power return for CCFL



## 6.0 Optical/FOS Measurement:

This spec generally employs the VESA Flat Panel Display Measurements Standard, Version 2 for its panel optical measurement procedures. Some measurement procedures, however, have been modified slightly to make them more meaningful to the end user. The procedure for measuring each of the following optical/FOS (Front Of Screen) properties are defined in this section.

- Luminance
- Contrast Ratio
- Uniformity
- Color Gamut
- Color Gamma
- Viewing Angle
- Response Time
- Residual Image

### 6.1 General Measurement Requirements:

#### 6.1.1 Measurement equipment.

Display FOS properties are measured with a photometer equivalent to a, Photo Research PR-650/880 or a TOPCON BM5A. Other measurement equipment with a larger luminance measurement tolerance,  $> \pm 2\%$ , or color tolerance  $> \pm 0.0015$  (1931 C.I.E.), will show approximate properties but should not be used to accurately compare measurements of one panel with another.

#### 6.1.2 Measurement environment.

Measurements are made in normal office condition environment. Measurements made outside these conditions may not be valid for comparison of one panel to another. The standard office conditions are.

Temperature:	$23^{\circ}\text{C} \pm 4^{\circ}\text{C}$
Humidity:	25% - 85% RH, non-condensing
Atmospheric pressure:	25 inHg to 31 inHg

#### 6.1.3 CCFL (Cold Cathode Fluorescent Lamp) warm-up time.

The CCFL requires time to achieve its set brightness after turn on. To insure accurate optical measurements the CCFL should be turned on and be allowed to warm-up for a minimum of 20 minutes.

#### 6.1.4 Darkroom measurement conditions.

To eliminate variation in screen reflection, all measurements should be performed in a darkroom,  $\leq 1$  lux. The darkroom definition assumes that all light comes from the display and that there are no reflective surfaces (white clothing, computer displays, light colored objects, etc.) that could corrupt the measurements.

#### 6.1.5 Display luminance control during measurement.

During a set of optical measurements the screen luminance should not be changed. Changing the luminance to optimize measurement is not allowed. Changes in luminance require that the entire FOS measurement suite be repeated.

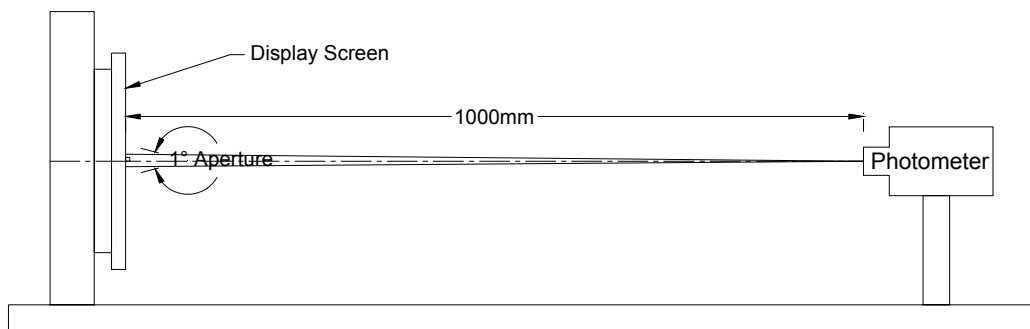
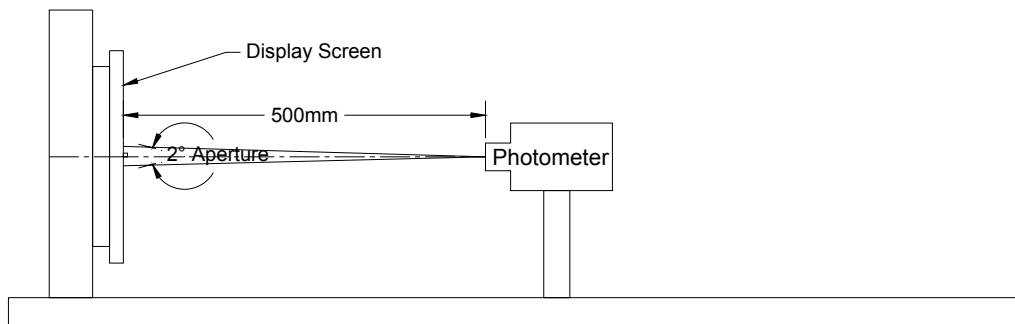
#### 6.1.6 Measurement viewing direction.

Luminance, contrast ratio, uniformity, color gamma, color gamut, and response time measurements should be performed with a viewing direction which is perpendicular,  $\pm 0.3^\circ$ , to the display screen.

Viewing angle measurements should be performed at angles that reference the screen center.

#### 6.1.7 Measurement equipment setup:

The photometer is placed at a fixed distance from the display screen to be measured. The fixed distance is determined by the photometer measurement aperture used. A  $2^\circ$  aperture is used when the photometer is positioned 500mm from the screen to be measured and a  $1^\circ$  aperture when the distance is 1000mm. "Normal" measurements are performed perpendicular to the display screen surface. See the drawings below.



## Example of a Typical Optical FOS Measurement System

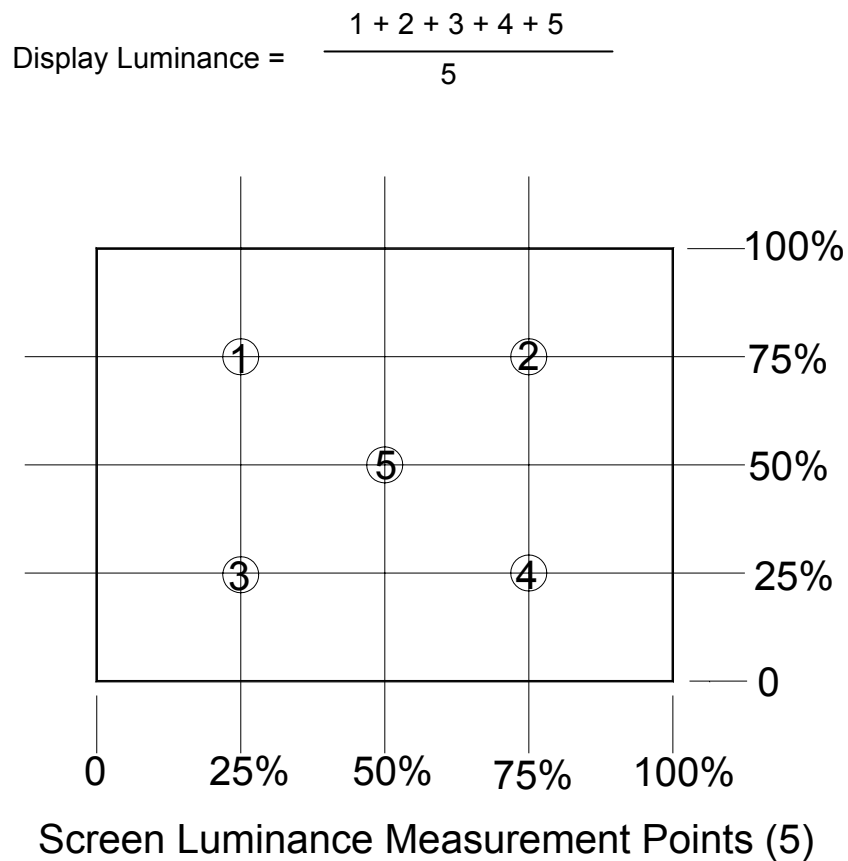


## 6.2 Luminance Measurement:

Luminance is a  $\text{cd/m}^2$  (nits) measurement of the display's white color (white screen).

To eliminate variations in environmental lighting conditions that can affect display luminance, all measurements are performed in a dark ambient.

Display luminance is defined as the average value of five (5) white screen measurements. The location of these 5 measurement points is shown in the drawing below.



### 6.3 Contrast Ratio Measurement:

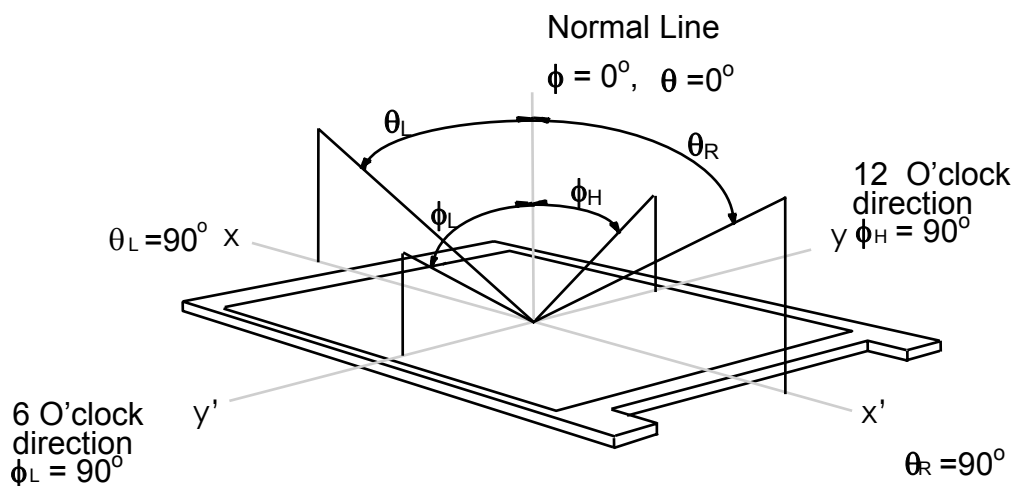
Contrast Ratio (CR) is the comparison of the display screen's maximum white luminance (white screen) to its minimum luminance (black screen).

CR is expressed as a ratio of white luminance value to black. Example: 150:1 (white luminance is 150 times greater than black luminance).

Contrast Ratio is measured perpendicular to the display at the screen center ("Normal Line",  $0^\circ$ ,  $0^\circ$ ).

A full white screen and a full black screen are used when measuring luminance for contrast ratio. Although other screen patterns (various black and white checkerboard patterns) could be used these can add variation to the CR value.

$$CR = \frac{\text{Luminance of all white screen}}{\text{Luminance of all black screen}}$$



## 6.4 White Uniformity Measurement:

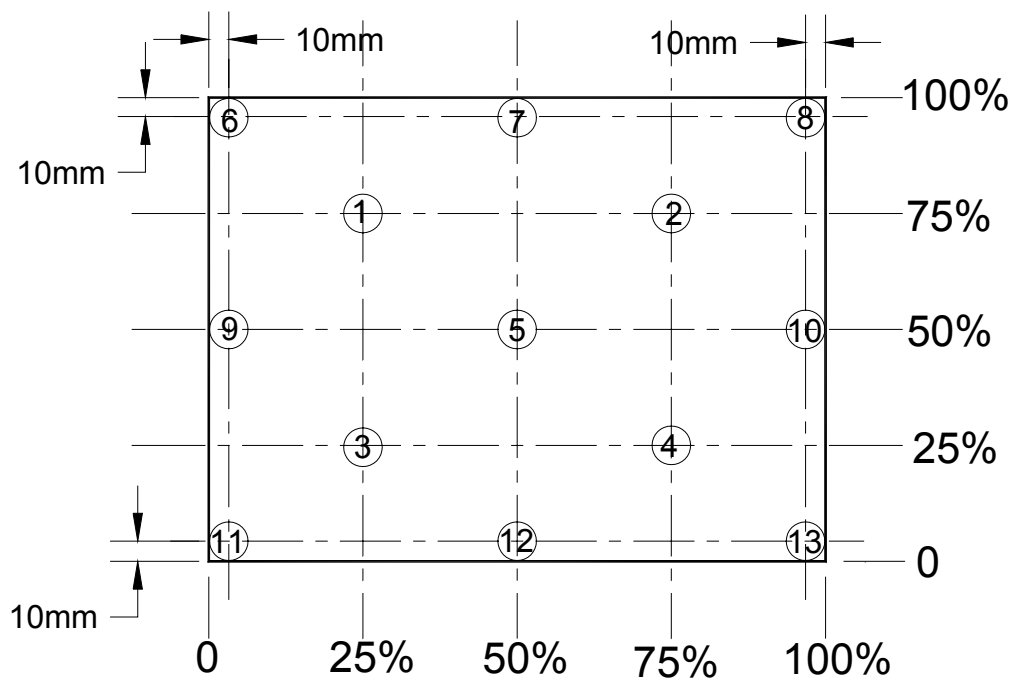
White luminance uniformity is a  $\text{cd/m}^2$  (nits) measurement of the display's white color across the display screen. This measurement describes the uniformity of the LCD lighting system.

To eliminate variations in environmental lighting conditions that can affect display luminance, all measurements are performed in a dark ambient.

All measurements are performed with the photometer perpendicular to the display screen surface.

Display luminance uniformity is defined as the percent (%) of luminance value variation over thirteen (13) white screen measurements. The location of these 13 measurement points is shown in the drawing below.

$$\text{Luminance \% Uniformity} = \frac{\text{Max Luminance (13 Pts., 1-13)} - \text{Min Luminance (13 Pts. 1-13)}}{\text{Max Luminance (13 Pts. 1-13)}}$$



Screen Uniformity Measurement Points (13)

## 6.5 Color Gamut Measurement:

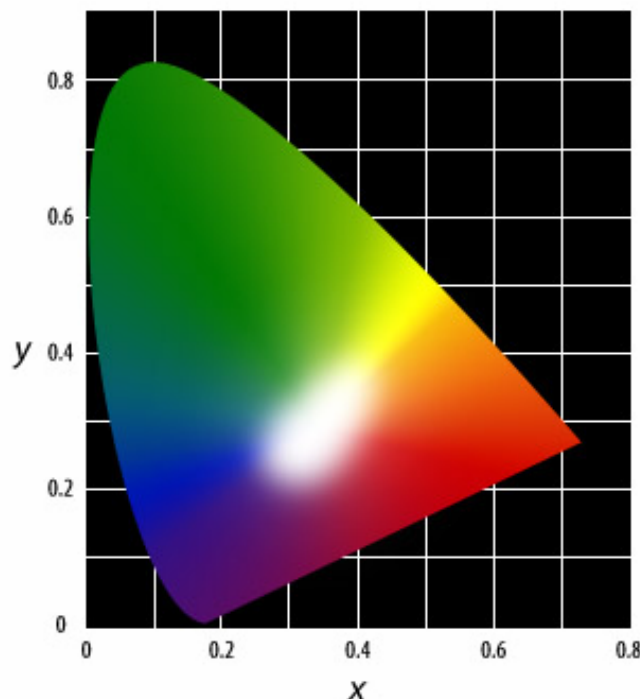
Color Gamut is the measurement of the display color chromaticity coordinates, referenced to the 1931/1976 CIE color standard, for its primary colors, red, green, and blue. These charts are shown below for reference only.

The measurements are taken at the screen center (Normal Line) perpendicular to the display. A 100% red screen ( $r=255$ ,  $g=0$ , &  $b=0$ ) is used to measure the color red. A 100% green screen ( $r=0$ ,  $g=255$ , &  $b=0$ ) is used to measure the color green. A 100% blue screen ( $r=0$ ,  $g=0$ , &  $b=255$ ) is used to measure the color blue.

Note: Graphic adapters typically define 8 bit color settings with 256 shades of gray for each color as shown above. Notebook panels are 6 bit and actually produce only 64 shades of gray for each color.

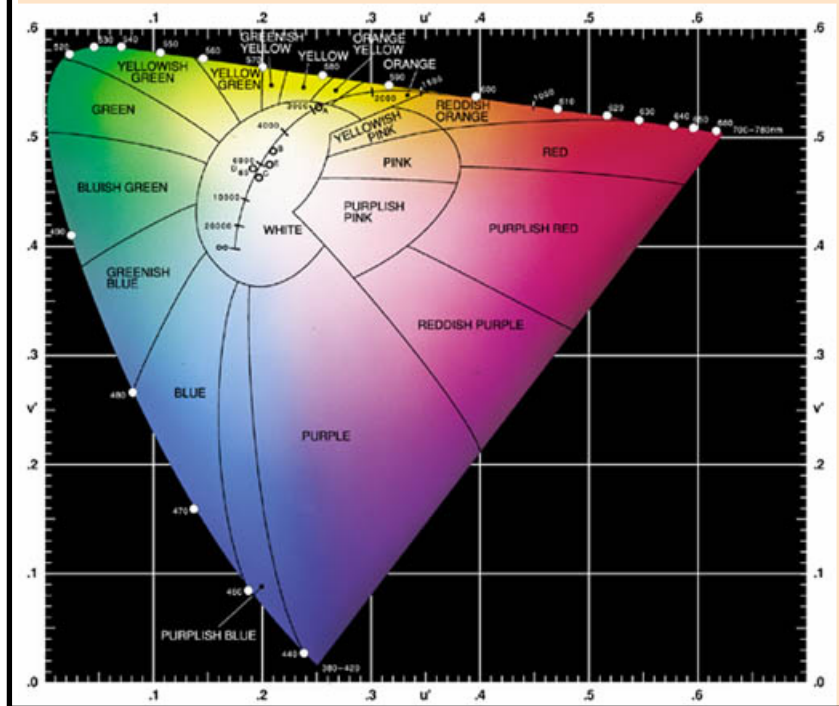
The area of the triangle formed on the CIE color chart, by the R G B coordinates, can be compared with the area of the NTSC color coordinate triangle. This comparison is typically made as the measured display's percentage of the NTSC standard. This percentage is commonly referred to as the color gamut for the display.

The chromaticity coordinates are used in conjunction with a chromaticity diagram, the most familiar one being CIE's 1931  $xyY$  Chromaticity Diagram:



The horseshoe-shaped color space is set in a grid using the chromaticity coordinates  $x$  and  $y$  as a locator for any value of hue and chroma. These correspond to the color itself (e.g., reddish-orange) and the fullness of the color or saturation. The coordinate  $z$  is not used, but can be inferred from the other two since the sum of the coordinates  $x + y + z$  is always 1.

## The 1976 CIE Chromaticity Diagram





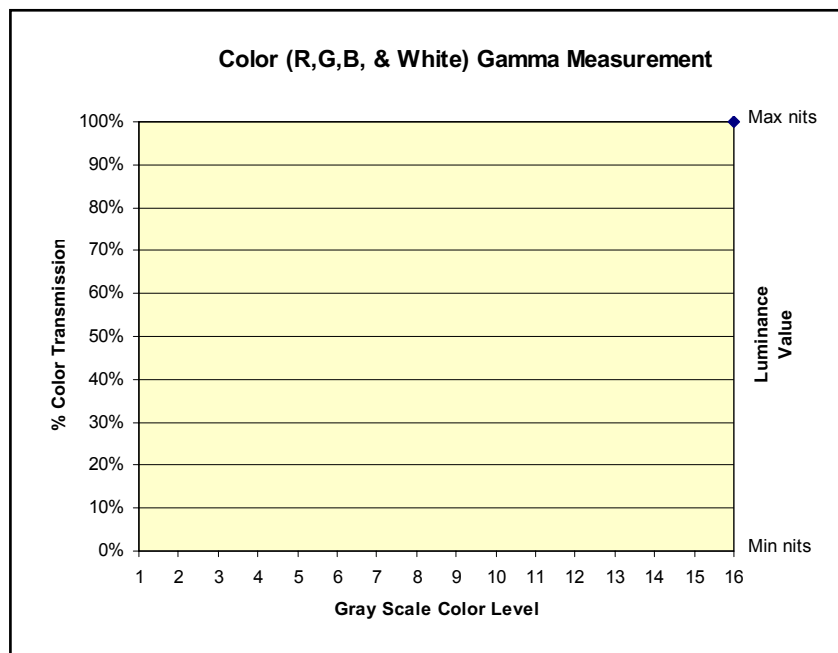
## 6.6 Color Gamma Measurement:

Color gamma is the measurement of Red, Green, Blue and White over their gray scale range (luminance transmission 0 – 100%). A minimum of 16 measurements for each color should be made. Note: Notebook display panels have a range of 64 shades of gray for each color, R G B & White.

The color gamma measurements are taken at the screen center (Normal Line) perpendicular to the display. The measurement units are nits ( $\text{cd/m}^2$ ) and are converted to percent (%) transmission and recorded in chart form. A sample chart format is shown below. A windows standard 2.2 gamma should be used.

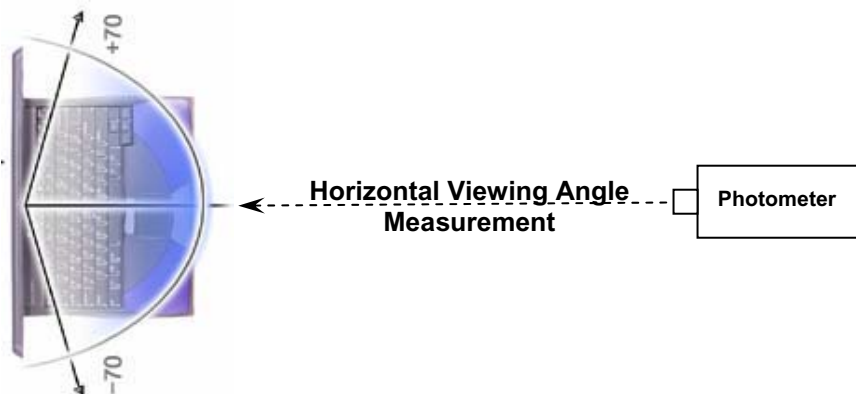
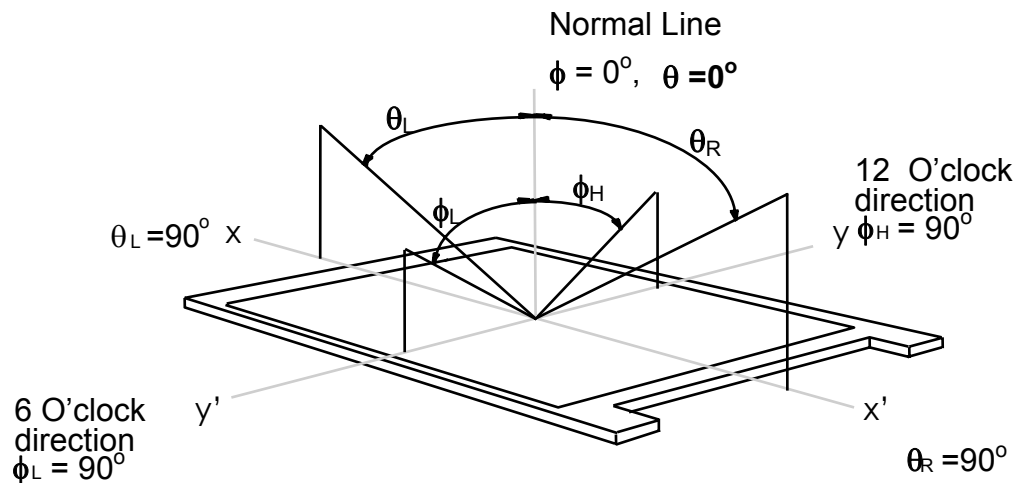
**Gray Scale Measurement Levels**

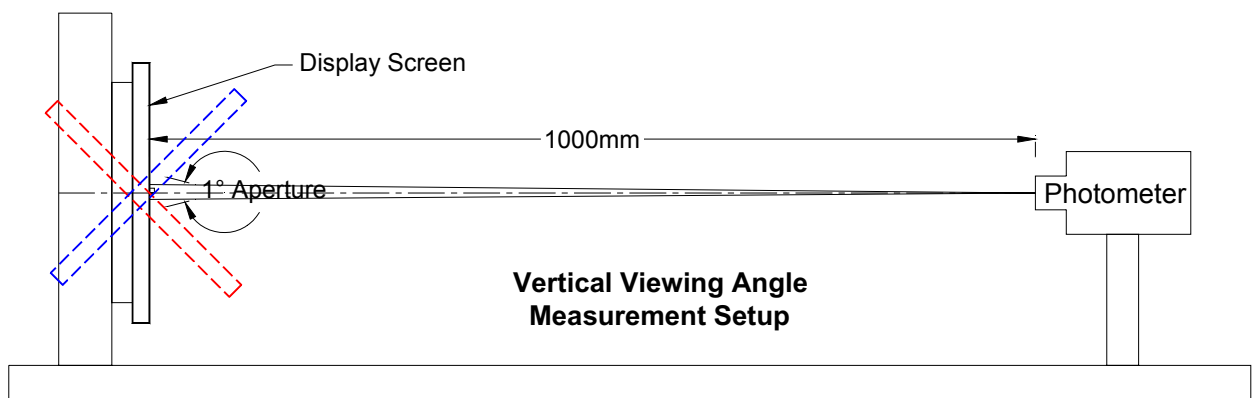
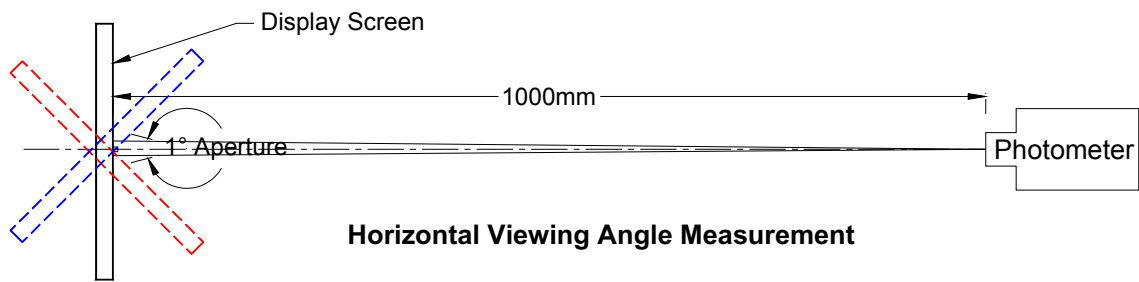
Gray Shade	Transmission or Gray Level	Measured Luminance	Gray Shade	Transmission or Gray Scale	Measured Luminance
1	0%, L0		9	53%, L34	
2	7%, L5		10	60%, L38	
3	13%, L9		11	67%, L42	
4	20%, L13		12	73%, L47	
5	27%, L17		13	80%, L50	
6	33%, L21		14	87%, L55	
7	40%, L26		15	93%, L59	
8	47%, L30		16	100%, L63	



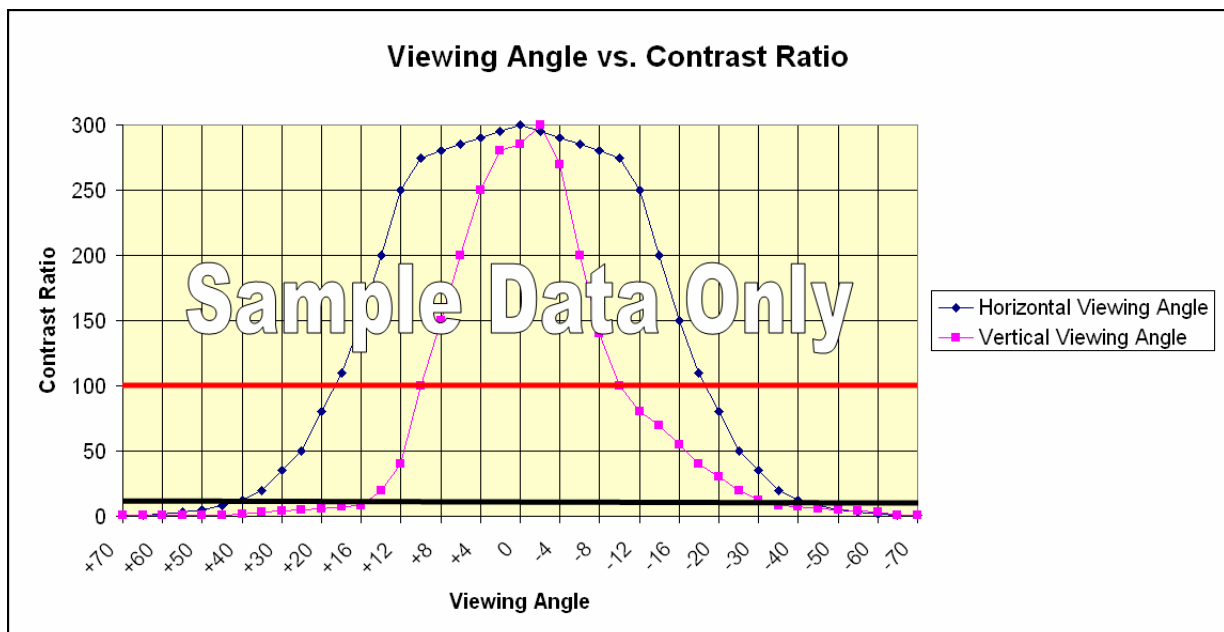
## 6.7 Viewing Angle Measurement:

Viewing angle is the measurement of contrast ratio, at the screen center, over a  $180^\circ$  horizontal and  $180^\circ$  vertical range (off-normal viewing angles). The  $180^\circ$  viewing angle range is broken down as follows;  $90^\circ$  ( $\theta$ ) horizontal left and right and  $90^\circ$  ( $\Phi$ ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.





Luminance measurements are made at a minimum of 20 viewing angles in both horizontal and vertical axis. The measurements are made on both white and black screens. Contrast Ratios are calculated and plotted per the graph below.

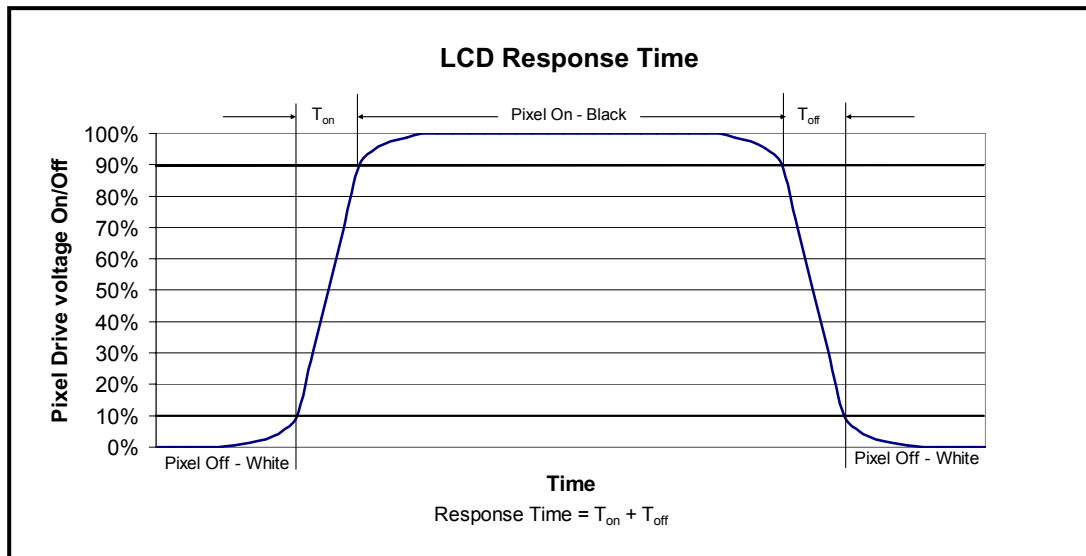


Viewing angles above  $\pm 20^\circ$  are measured in  $10^\circ$  increments. Viewing angles below  $\pm 20^\circ$  are measured at  $4^\circ$  increments.

Viewing angles are typically specified as a maximum  $\pm$  angle with a Contrast Ratio greater ( $\geq$ ) than 10:1. Consumers, however, expect useable viewing angles to have a Contrast Ratio's greater ( $\geq$ ) than 100:1. Plotting the horizontal and vertical viewing angles in the chart format above provides an easy to understand process for evaluating and comparing display panels.

## 6.8 Response Time Measurement:

Response time is the measurement of the total time takes to turn a pixel “On” and “Off”. A pixel is determined to be “On” when its drive voltage reaches 90% of maximum and “Off” when the voltage level drops to 10%. “On” and “Off” are also referred to as “Rise” and “Fall” times. See the chart below.



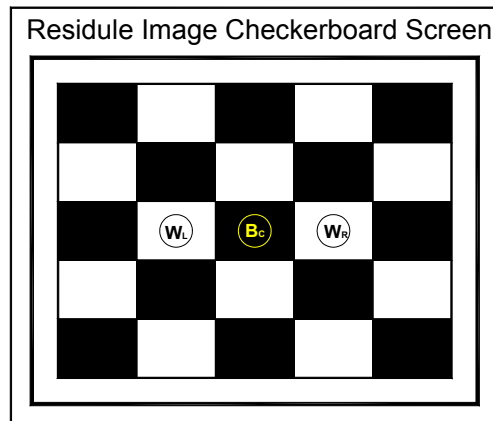
Black and White screen patterns are switched and the resulting electro-optical step response function is measured. Measurements are made at the screen center perpendicular to the display surface (Normal Line). The photometer must have a response time and sample rate  $\leq 0.1$  the total response time,  $T_{On} + T_{Off}$ . The photometer is connected to a computer or storage oscilloscope which collects the sample data and processes it to display the “Total LCD Response Time”.

In LCD display screens with slower response times, a fast moving screen image can appear blurred if it moves faster than the screen can update the pixels. A black box moving across the screen at different speeds can be an indicator of the display screen’s response time. The leading and trailing edge of the box will appear blurred if the speed of its movement is faster than display can update its pixels. While this is not an accurate measurement of screen response time it can be used to generally compare the speed of one panel with another. Updates to pixel drive technology can improve the apparent response time without changing the display’s physical internal design/technology.

## 6.9 Residual Image Measurement:

A residual or retained screen image may occur if a fixed screen pattern is displayed for a long period of time. This residual image should dissipate after a short time.

A 5 x 5 black and white checkerboard pattern should be used for the measurement (FPDMSU.ppt, slide #90 from the VESA file "Flat Panel Display Monitor Setup Patterns", FPDMSU.ppt.). Initial luminance measurements are made on the checkerboard screen center squares per the drawing below.



The checkerboard pattern is allowed to remain on the screen (burn in) for 16 hours.

After the burn in period (16 hours) the screen pattern is changed to all white. Notebook displays are "normally white" screens so this turns off all the TFT pixels.

The white screen is allowed to remain on for 2 minutes.

After the 2 minutes has elapsed, measure the white screen luminance in the same locations as on the original checkerboard pattern.

Compare the original checkerboard contrast ratio (CR) with the 2 minute post burn in measurement.

$$\text{Initial checkerboard CR} = \frac{(W_L + W_R)/2}{B_C}$$

$$\text{White screen post burn in CR} = \frac{(W_L + W_R)/2}{B_C}$$

The second CR measurement, white screen post burn in, should be a specified percentage (%) of the initial checkerboard CR. This percentage value is determined by individual panel specifications but will typically be  $\leq 1\%$ .

A 2 minute post burn in (white screen) CR measurement, as described above, can also be used to develop a test limit for a residual image specification.

## 7.0 Power Measurement:

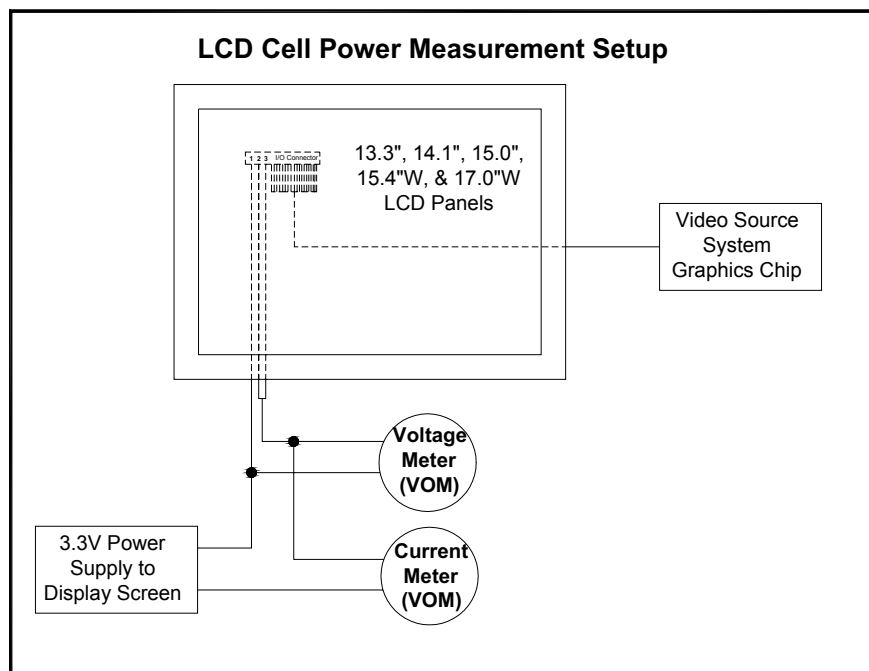
Display panel power is the summation of the LCD cell + the backlamp. The LCD cell is powered by a  $3.3V \pm 10\%$  supply from the notebook system. The backlamp CCFL (Cold Cathode Fluorescent Lamp) is driven by a high voltage inverter which is powered by a 5V supply from the notebook system. Measurements for the LCD cell and the backlamp/inverter are measured separately and the results are totaled to define the display module's power.

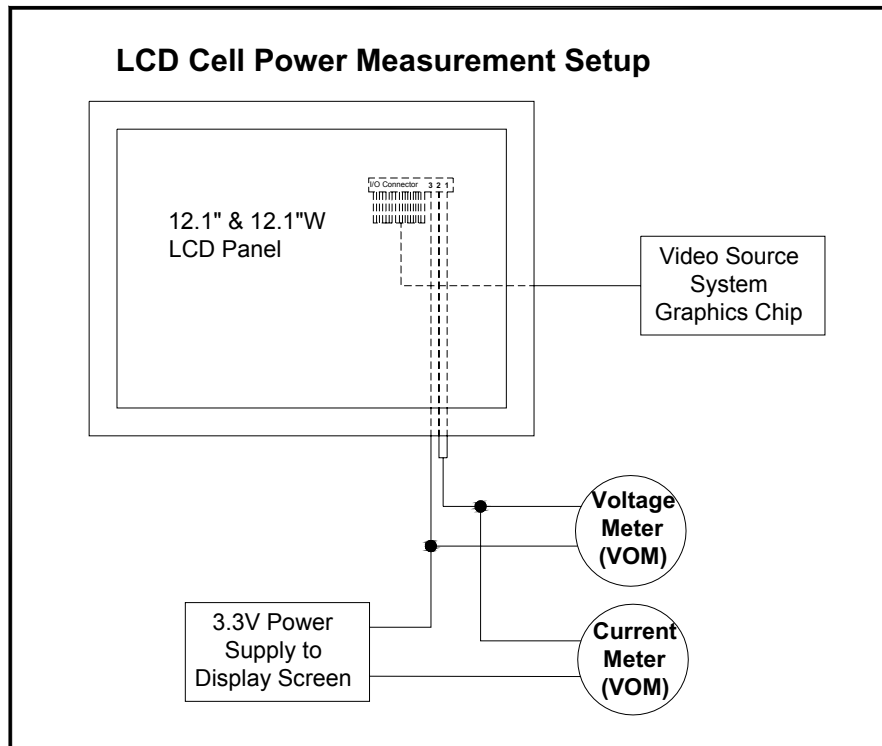
The procedures defined here basically mirror those established by the EBL WG (Extended Battery Life Working Group), [www.eblwg.org](http://www.eblwg.org). Power measurement assumes that the panel is powered from a power source separate from the LCD panel. Display power(P) for both the LCD cell and backlight is defined as the product of the input voltage (V) and its current (I) draw,  $P=VI$ . The power unit is Watts.

LCD and cell and Backlamp measurements can be performed using a Fluke NetDaq Data Acquisition (Model 2645A), Fluke 87 III multimeter, or the equivalent.

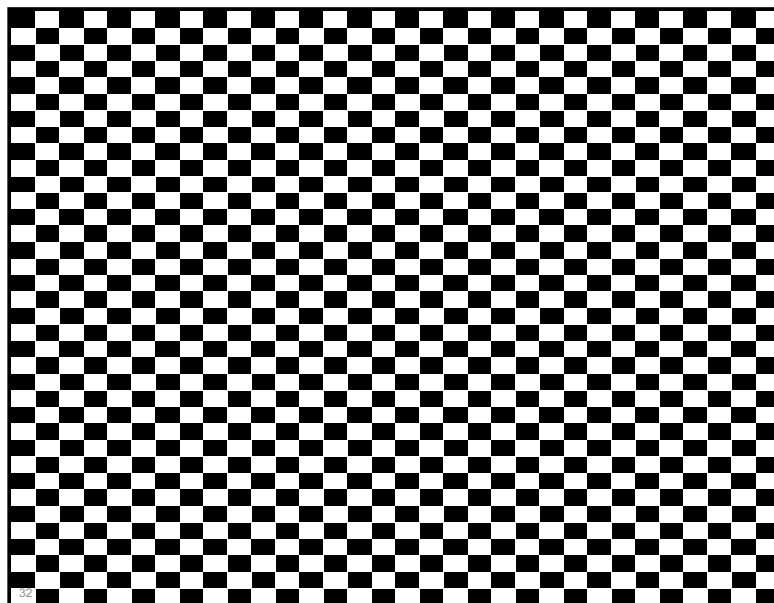
### 7.1 LCD Cell Power Measurement:

The panel's luminance, produced by the backlight, has no impact on the LCD cell power measurement. The power supply connections are made directly to the display's I/O connector pins or to the equivalent location at a system cable termination. For 12.1" single channel LVDS panels, power (3.3V) is supplied through pins 1 and 2. Pin 3 is a 12.1" panel ground. 14.1" – 17.0" 2 channel LVDS panels have pin 2 and 3 designated as "power (3.3V) in". Pin 1 is a 14.1" – 17.0" panel ground. The basic panel power test setups are shown below.





The display cell power varies according to the pattern being displayed on the screen. To eliminate variables in measurement, the screen pattern is fixed as a checkerboard. This pattern provides a typical screen for power measurement. The pattern used is a black and white 32 x 36 checkerboard, slide #100 from the VESA file "Flat Panel Display Monitor Setup Patterns", FPDMSU.ppt. This file is available at the VESA website, [www.vesa.org](http://www.vesa.org).



32 x 36 Black & White Checkerboard Pattern



## 7.2 **Backlamp Power Measurement:**

The backlamp is driven by an inverter which can be either notebook system supplied or part of a LCD panel module. In either case the true power required to drive the backlamp is a measurement of the inverter input. The efficiency of the inverter and total backlighting system will greatly affect the backlamp power usage. The backlamp power measurement process is the same for all LCD panel sizes. Backlamp power usage is in direct proportion to the panel luminance. As panel luminance increases power also increases. For this reason it is necessary that a standard luminance levels be defined for measurement. These standard luminance levels allow backlamp power comparisons of one panel to another. Two (2) luminance levels are defined for backlamp power measurement.

Level one (1) is the maximum LCD panel luminance. In notebook products this luminance level is typically used with AC system power input. Since the notebook user can set the panel luminance manually, power measurement at this level is required.

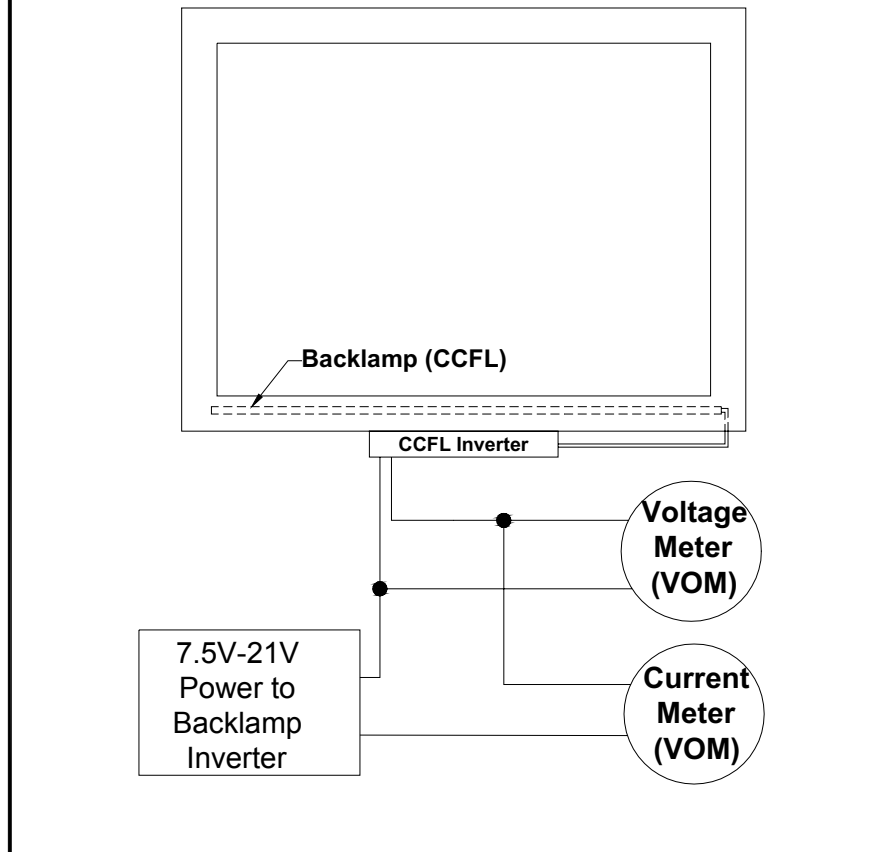
Under battery operation most notebook systems are initially set to optimize battery life and at the same time provide an adequate level of panel luminance. This battery luminance level is typically  $\sim 60\text{nits (cd/m}^2\text{)}$ . The second (2) luminance level for backlamp power measurement is therefore set manually at  $\sim 60\text{nits}$ . 60nits will typically be an approximate preset luminance level in the notebook system.

The backlamp measurement procedure requires that the panel luminance be measured and manually set. First, set the LCD panel to "Luminance Level 1" and measure the inverter input voltage and current draw. Second, set the LCD panel to "Luminance Level 2" and measure the inverter input voltage and current draw. The power is again the product of the voltage and current,  $P=VI$ . See the setup drawing below.

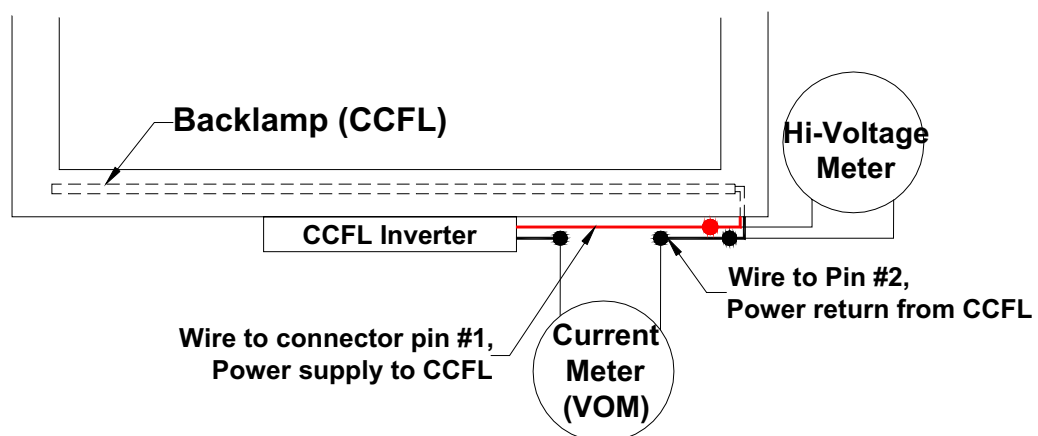
Backlamp measurements can performed using with a Fluke 87 III digital multimeter or the equivalent.

The backlamp power can be measured without the inverter as shown below. The power is again the product of the voltage and current,  $P=VI$

## LCD Backlamp (CCFL) with Inverter Power Measurement Setup



## LCD Backlamp Only (CCFL) Power Measurement Setup



## 8.0 Inverter Integration:

This section is optional but is highly recommended.

Backlamp inverters can be integrated to the LCD panel module. This provides for true panel interchangeability from one LCD supplier to another. This also insures optimized compatibility between the inverter and the LCD panel.

Inverter integration to the LCD panel requires that the inverter dimensions, location, connector type and location, and I/O pin-outs be defined for all size panels. 12.1"W, 13.3", 14.1", 15.0", 15.4"W, and 17.0"W use a 20-pin inverter input connector. The 14.1W panel uses a 12-pin inverter input connector.

The inverter locations and the input pin-outs are shown in the charts and drawings below.

### 8.1 Inverter Input Connectors

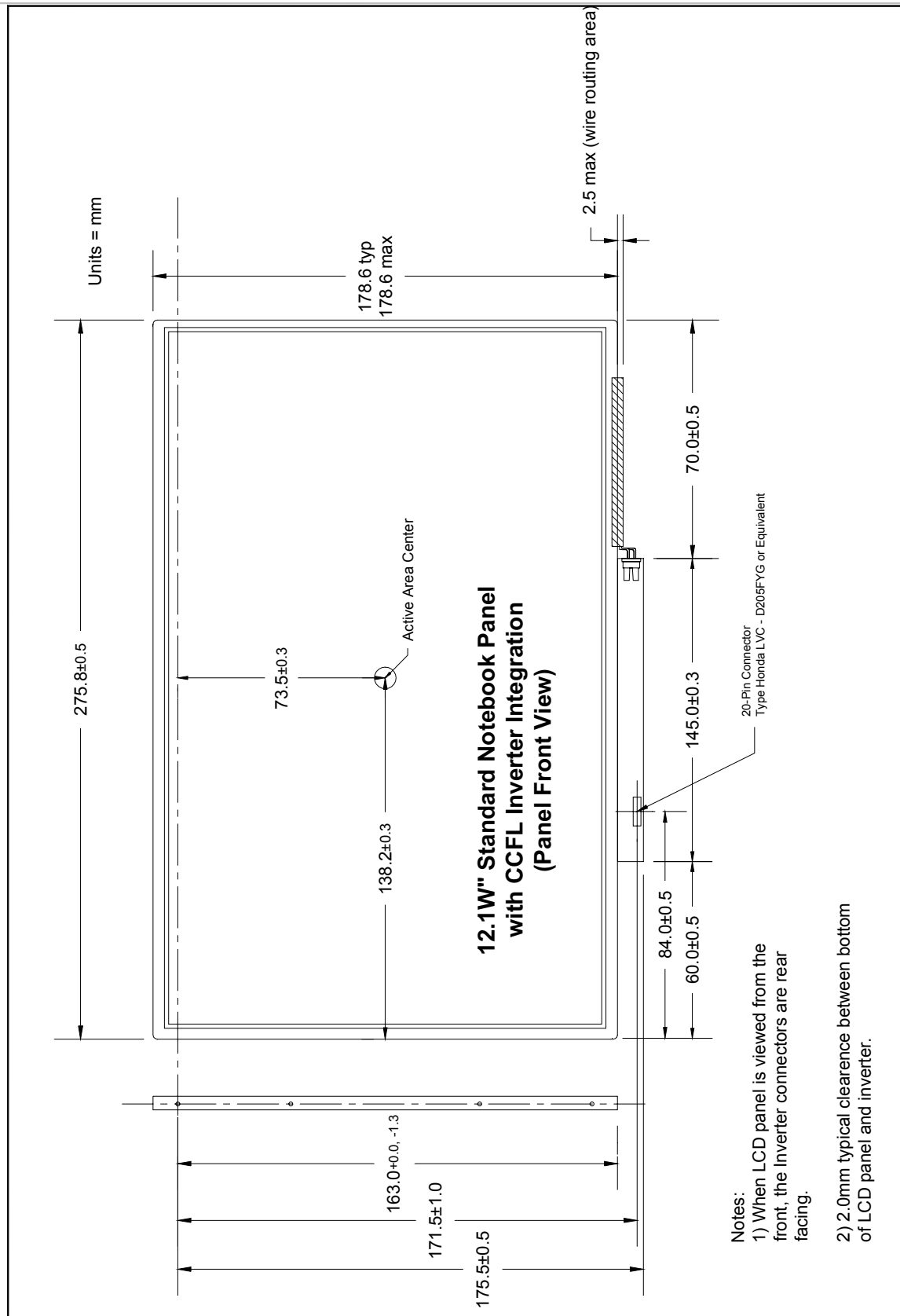
#### 8.1.1. 12.1"W, 13.3", 14.1", 15.0" 15.4'W, and 17.0W" Inverter Input Connector Pin-Out

Input connector		Voltage	Comments
Honda LVC-D20SFYG or equivalent			
Pin	Function		
1	INV_SRC	7.5V to 21V	This power rail should be used as a power rail to drive the backlight DC-AC converter
2	INV_SRC	7.5V to 21V	This power rail should be used as a power rail to drive the backlight DC-AC converter
3	INV_SRC	7.5V to 21V	This power rail should be used as a power rail to drive the backlight DC-AC converter
4	NC	-	No Connection
5	GND	0V	Ground
6	NC	-	No Connection
7	5VALW	5V	This should be used as power source for the control circuitry on the inverter and stores the brightness/contrast values & the circuit that interfaces with SMB_CLK & SMB_DAT
8	GND	0V	Ground
9	SMB_DAT		SMBus interface for sending brightness & contrast information to the inverter/panel
10	SMB_CLK		SMBus interface for sending brightness & contrast information to the inverter/panel
11	GND	0V	Ground
12	FPBACK		Control signal input into the inverter to turn the backlight ON & OFF (1 - ON, 0 – OFF)
13	GND	0V	Ground
14	LAMP_STAT		Lamp status (Feedback, Lamp On = 5v, Lamp Off 0v), from control chip
15 ~ 20	NC	-	No Connection

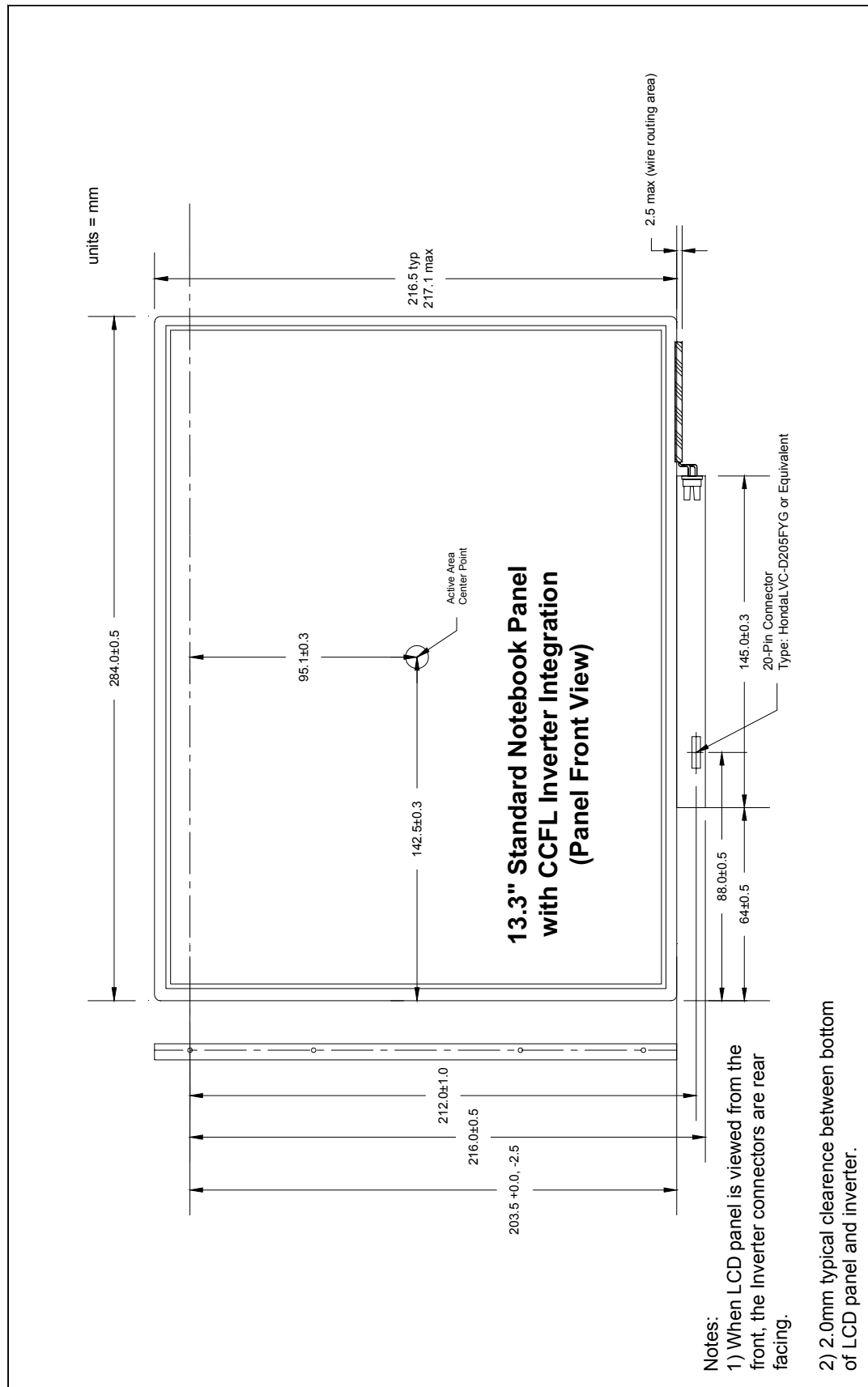
**8.1.2. 14.1"W Inverter Input Connector Pin-Out**

Input connector		Voltage	Comments
JAE FI-K12SL-VF or equivalent			
Pin	Function		
1	INV_SRC	7.0V to 21V	This power rail should be used as a power rail to drive the backlight DC-AC converter
2	INV_SRC	7.0V to 21V	This power rail should be used as a power rail to drive the backlight DC-AC converter
3	INV_SRC	7.0V to 21V	This power rail should be used as a power rail to drive the backlight DC-AC converter
4	5VALW	5V	This should be used as power source for the control circuitry on the inverter and stores the brightness/contrast values & the circuit that interfaces with SMB_CLK & SMB_DAT
5	GND	0V	Ground
6	SMB_DAT		SMBus interface for sending brightness & contrast information to the inverter/panel
7	SMB_CLK		SMBus interface for sending brightness & contrast information to the inverter/panel
8	GND	0V	Ground
9	FPBACK		Control signal input into the inverter to turn the backlight ON & OFF (1 - ON, 0 – OFF) PWM Enable
10	GND	0V	Ground
11	PWM	Variable V	Pin used for PWM voltage input brightness control.
12	LAMP_STAT	0V/5V	Lamp status, used for panel diags, (Feedback, Lamp On = 5v, Lamp Off 0v), from control chip.

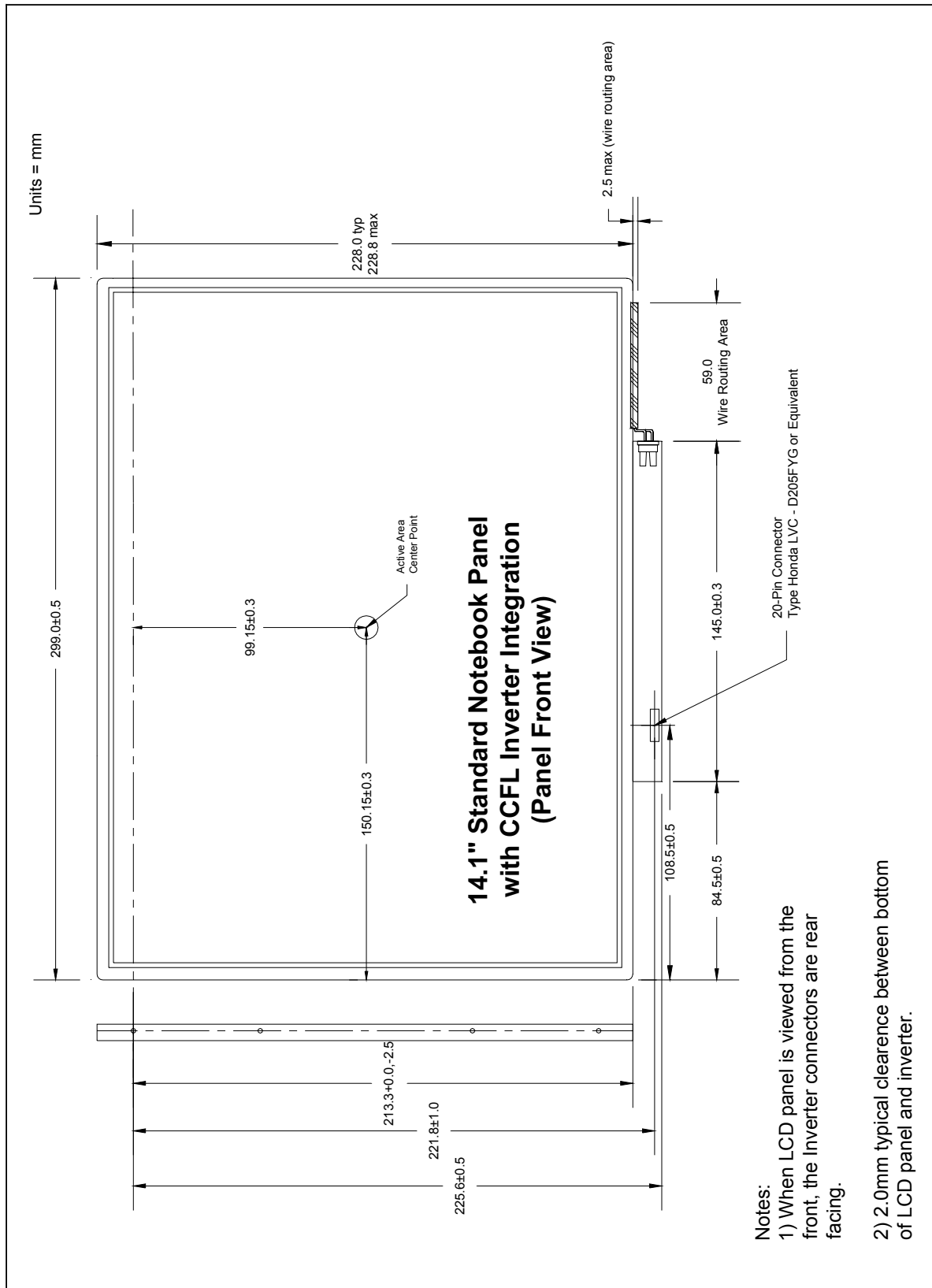
## 8.2 12.1"W Integrated Inverter Placement



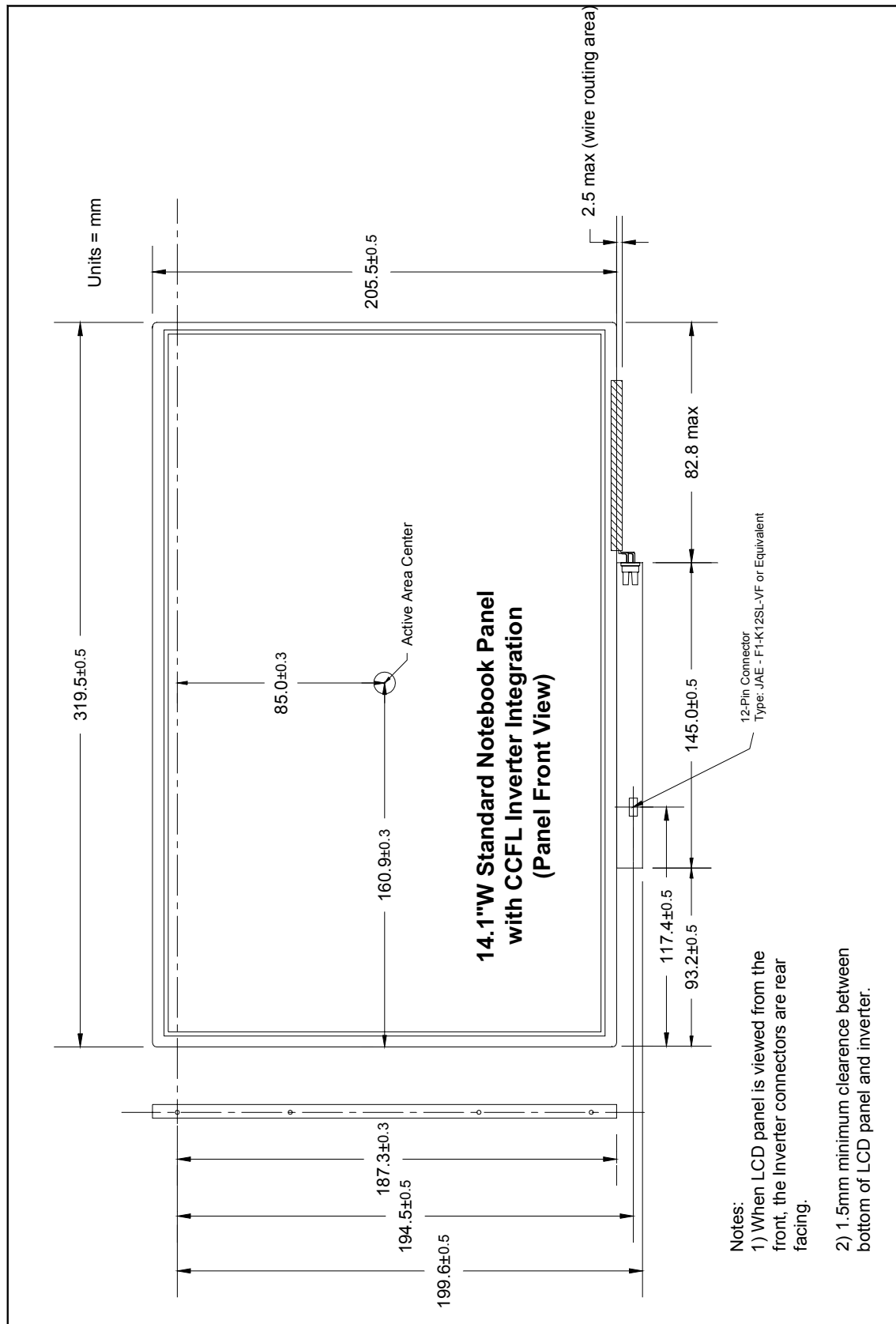
### 8.3 13.3" Integrated Inverter Placement



## 8.4 14.1" Integrated Inverter Placement

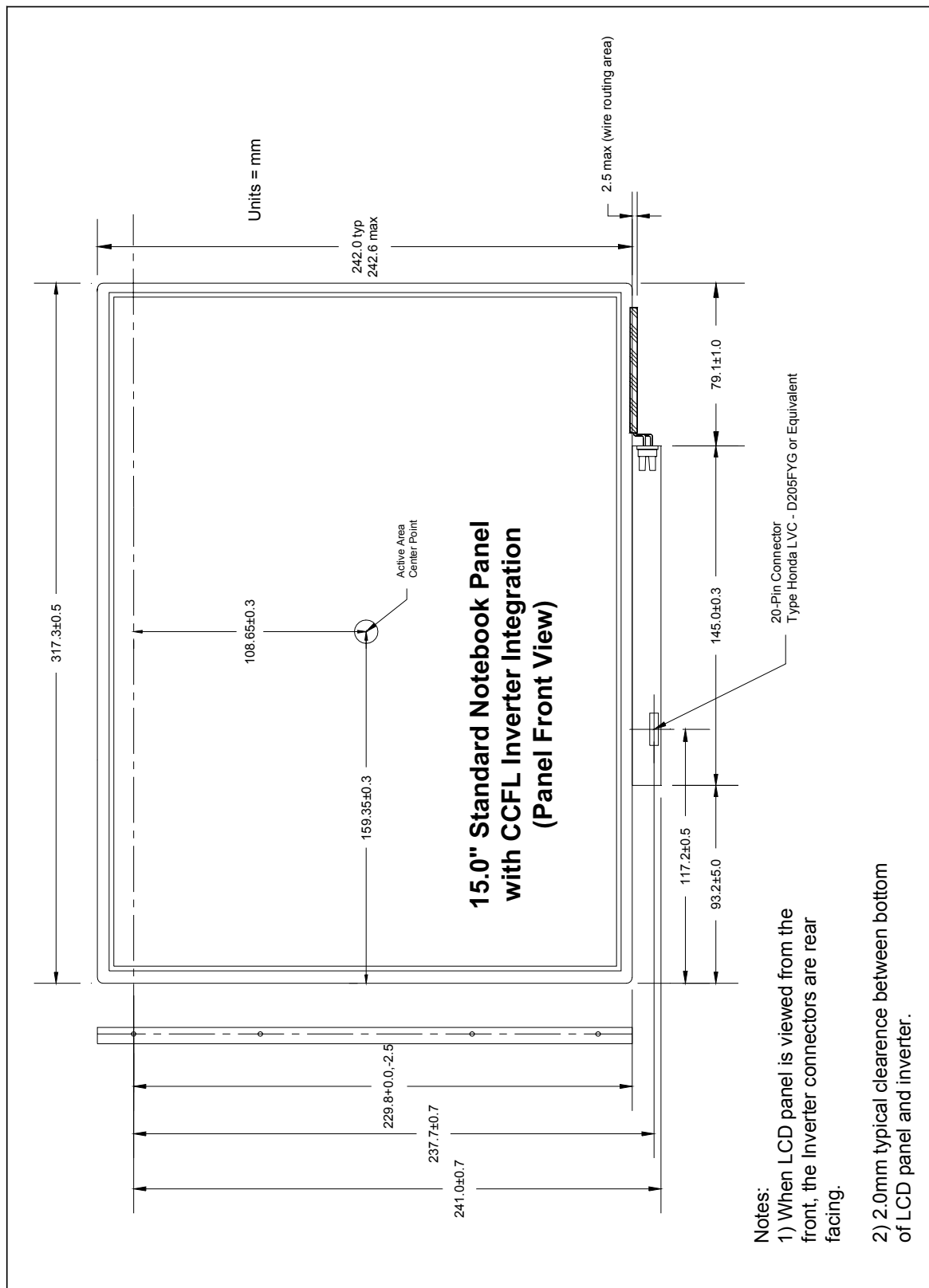


## 8.5 14.1"W Integrated Inverter Placement

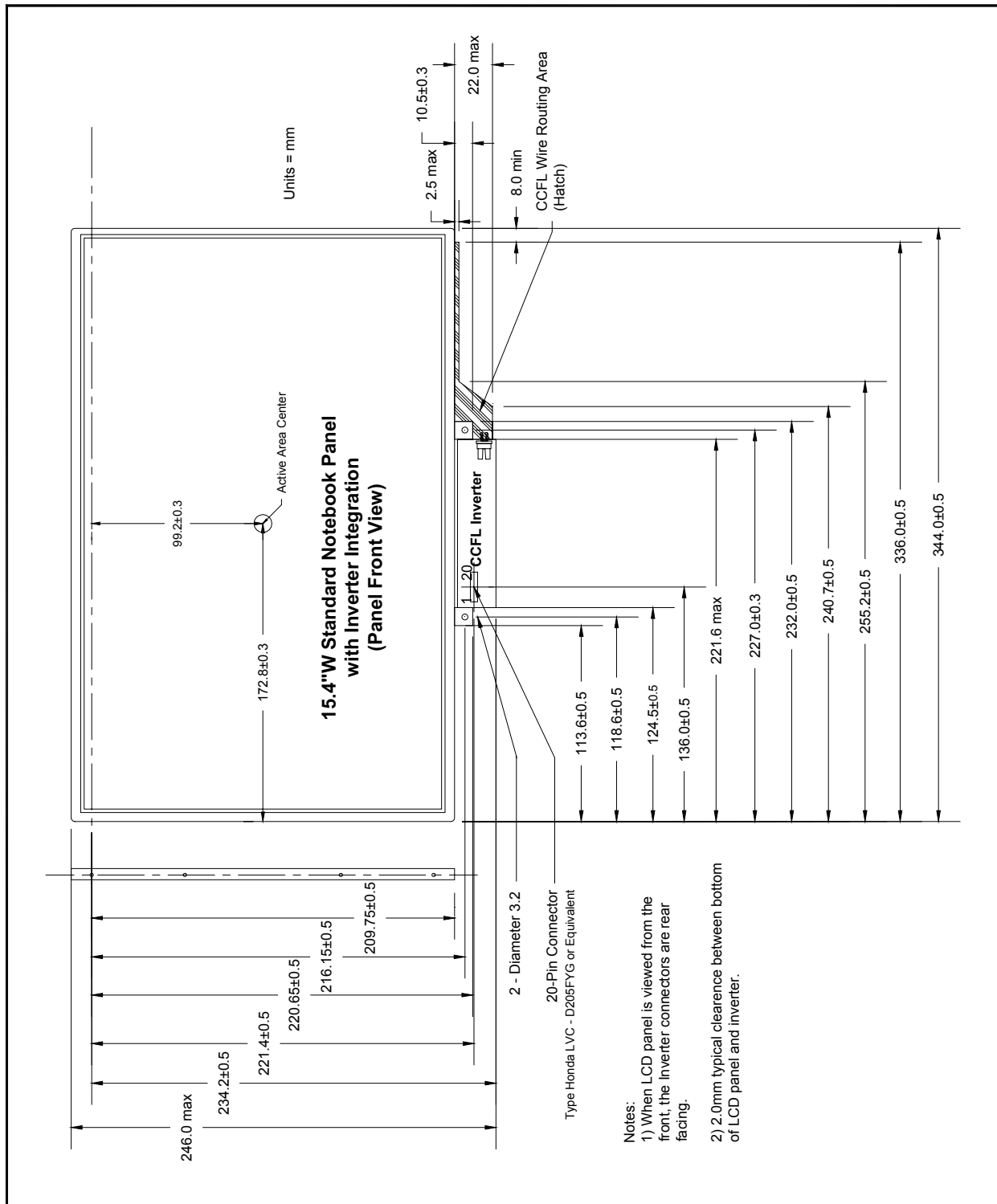




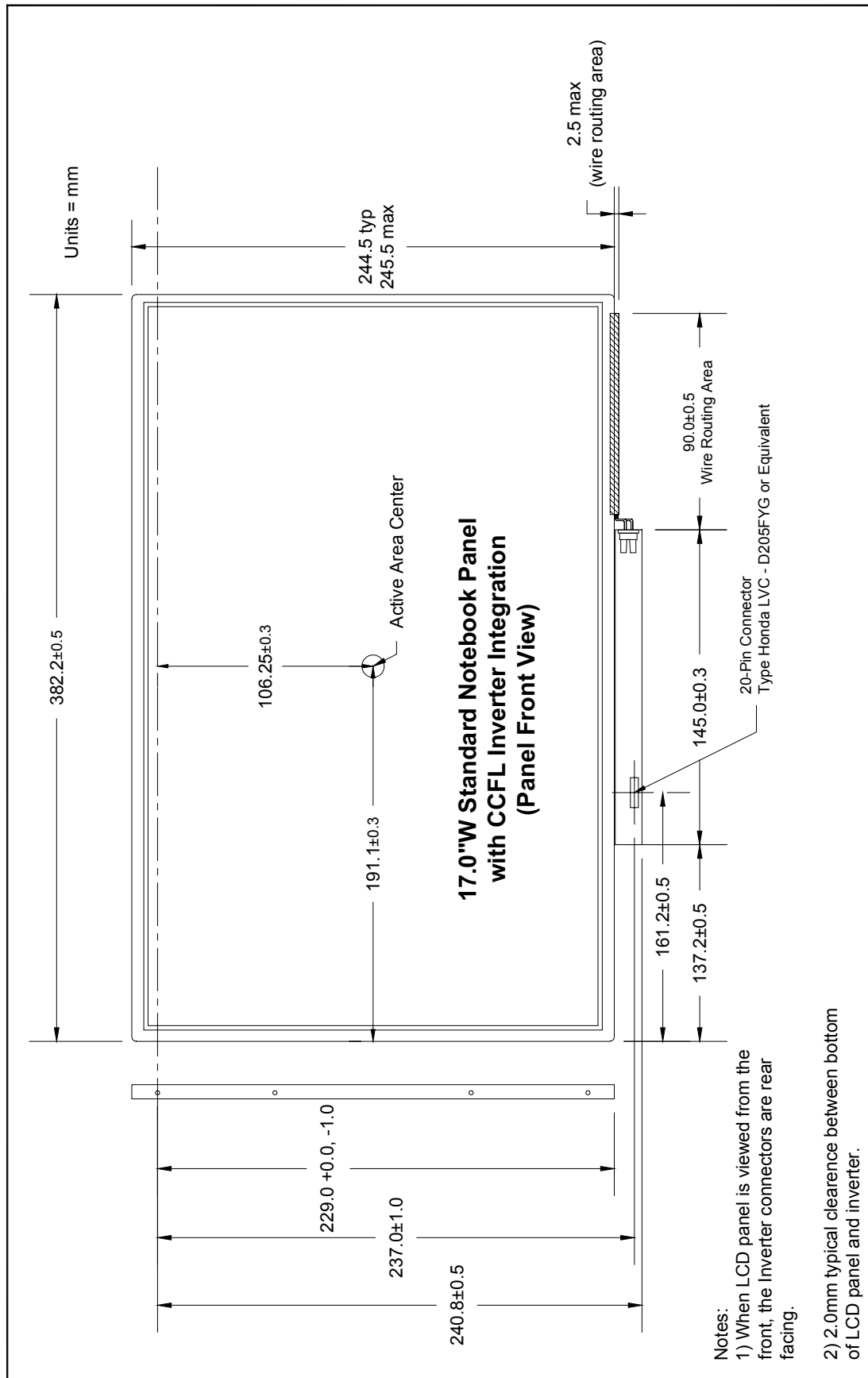
## 8.6 15.0" Integrated Inverter Placement



## 8.7 15.4" W Integrated Inverter Placement



## 8.8 17.0" W Integrated Inverter Placement



## 9.0 Screen Cosmetic Evaluation:

9.1 Display screen cosmetic evaluation limits are established by the PC maker and the LCD supplier. Those screen cosmetics for evaluation are defined below.

- 9.1.1 **Black Spots** – Minor Defect (Contamination in front polarizer layer) Spots that appear dark in the display pattern and vary/remain unchanged in terms of size and shade regardless of the adjustment of brightness or viewing angle. Defects are typically visible with the panel turned off but may, in some cases, be noticeable in white or 32 gray screens.
- 9.1.2 **Black Lines** – Minor Defect (Contamination in front polarizer layer) Lines that appear dark in the display pattern and vary/remain unchanged in terms of size and shade with the adjustment of brightness or viewing angle. Defects are typically visible with the panel turned off but may, in some cases, be noticeable in white or 32 gray screens.
- 9.1.3 **White Spots** – Minor Defect (Contamination in front polarizer layer) - Spots that appear light in the display pattern and vary/remain unchanged in terms of size and shade regardless of the adjustment of brightness or viewing angle. Defects are typically visible with the panel turned off but may, in some cases, be noticeable in black or 32 gray screens.
- 9.1.4 **White Lines** – Minor Defect (Contamination in front polarizer layer) Lines that appear light in the display pattern and vary/remain unchanged in terms of size and shade regardless of the adjustment of brightness or viewing angle. Defects are typically visible with the panel turned off but may, in some cases, be noticeable in black or 32 gray screens.
- 9.1.5 **Nap** – Minor Defect (Contamination in front or rear polarizer layers) This refers to fibrous material such as lint/hair within the display. Defects are typically visible with the panel turned off but may, in some cases, be noticeable in white or 32 gray screens
- 9.1.6 **Polarizer Scratches** – Minor Defect This refers to an actual scratch on the Polarizer (outside) surface.
- 9.1.7 **Polarizer Dents** – Minor Defect Dents are small indentations or impressions on the Polarizer (outside) surface.
- 9.1.8 **Rub** – Minor Defect This is an unevenness, or shiny spot, on the display surface where the anti-glare coating has been damaged or removed.
- 9.1.9 **Pixel Failure (Stuck On)** – Minor Defect within spec, Major Defect outside of spec limits This is a failure of the pixel on a TFT display; it is most often bright and will be a particular color.
- 9.1.10 **Pixel Failure (Stuck Off)** – Minor Defect within spec, Major Defect outside of spec limits This is a failure of the pixel on a TFT display; it is most often black and will be seen only on 32 gray or colored backgrounds.
- 9.1.11 **Line (Row / Column) Out** – Major Defect During operation the unit displays one or more horizontal or vertical lines in black, red, green, or blue patterns.
- 9.1.12 **Glass Crack** – Major Defect Refers to a fracture in a glass layer of the display

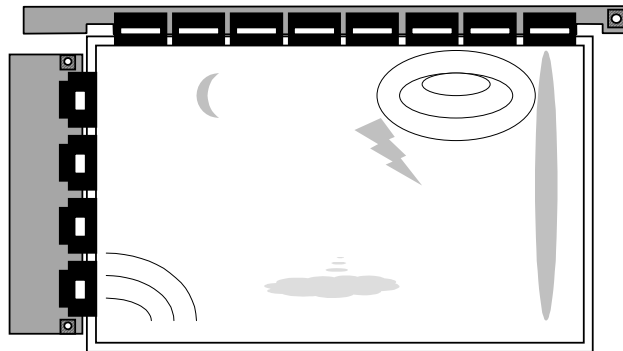
**9.1.13 White or black spots** – Minor Defect within spec, Major Defect outside of spec limits Refers to white or black spots visible within the glass cell only visible during panel operation, white, black, 32 gray, red, green, or blue screen patterns.

**9.1.14 Etch / TFT** – Major Defect Usually reflected as a failure of a part of a single row, or a column only visible during panel operation, black, red, green, or blue screen patterns

**9.1.15 Backlight** – Major Defect Backlight does not operate. Videotext is barely perceptible on the screen, and no light is visible along the edges of the LCD.

**9.1.16 LGP (Light Guide Pipe)** – Major Defect Panel operates but white scratch like lines are visible seen from an angle, or black spots that show up in all color display patterns. Typically caused by a crack in the plastic LGP portion of the backlight assembly.

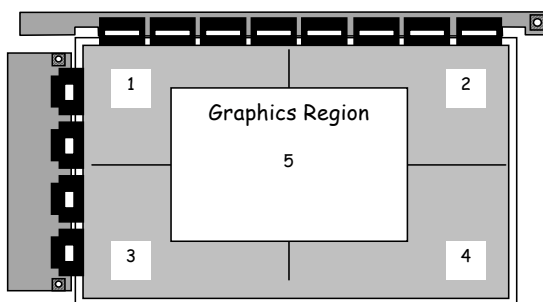
**9.1.17 Pooling / Ripple** - Minor Defect within spec, Major Defect outside of spec limits This caused by the displacement of spacers and liquid crystal (LC) material that result in a visible discoloration in the shape of wavy lines, circles (Newton Rings), spots, ½ moons, or other irregularities in the display pattern.



**9.1.18 Light Leak** – Minor Defect CCFL light leak at the edges of the screen outside of CR 10:1 viewing angles. Major Defect when CCFL light leak occurs within the CR10:1 viewing angle.

**9.2** Display screen cosmetic defects may be weighted by their location. The drawings below define these screen locations (quadrants).

Display Quadrants



LCD Size	Graphics Region Dimensions
12" – 13.9"	6" x 4"
14" – 15.4"	7" x 5"
17.0"	8" x 6"

Note: A clear plastic sheet with the display quadrants outlined can be used as a reference for checking defect location.

### 9.3 Cosmetic Visual Defects:

NOTE: Functional defects take precedence over visual.

Defect Type	Panel Type	Reject Size (mm) Reject Count (n)	Notes	Defect Severity
White / Black Spots (Contamination in/on front polarizer layer)	New panel or post reliability stress test	Dia > 0.7 mm n =>	1, 3	Minor Defect
White / Dark Lines & Nap (Contamination in/on front polarizer layer)	New panel or post reliability stress test	W > 0.7 mm L > 1.0 mm n =>	2, 3	Minor Defect
Polarizer Scratch	New panel	W > 0.4 mm L > 5.0 mm n =>	2	Minor Defect
Polarizer Scratch	Post reliability stress test	W > 0.4 mm L > 5.0 mm n =>	2	Minor Defect
Polarizer Dent	New panel	D > 0.5 mm n >	2	Minor Defect
Polarizer Dent	Post reliability stress test	D > 0.5 mm n >	2	Minor Defect
Newton Ring (Cell Internal)	New panel or post reliability stress test	Dia > 20 mm n =>	2, 3	Major Defect
Newton Ring (Cell Internal)	New panel or post reliability stress test	Dia > 20 mm n =>	2, 3	Major Defect
Rub Defect	New panel	Not Allowed	2	Minor Defect
Rub Defect	Post reliability stress test	Not Allowed	2	Minor Defect
Glass Crack	New panel or post reliability stress test	Not Allowed	2, 3	Major Defect
Polarizer delamination (Bubble)	New panel or post reliability stress test	>0.10 mm n >	2	Minor Defect
Total number for all major & minor defects	New panel or post reliability stress test	n =>		All Defect

Note 1: White/black spots are inspected within the panel viewing angles only

Note 2: Inspected with the panel turned off.

Note 3: Inspected with both a white and 32 level gray screen pattern.

#### 9.4 Screen Functional Defects:

Evaluated in Black, White, Red, Green, Blue, and 32 Gray screens.

NOTE: Functional defects take precedence over visual defects

Defect Type	Panel Type	Reject Size (mm) Reject Count (n)	Notes	Defect Severity
Bright Pixels – Random	New panel	n >	All Quadrants	Major Defect
Bright Pixels – Green	New panel	n >	All Quadrants	Major Defect
Bright Pixels – 2 Adjacent	New panel	n >	All Quadrants	Major Defect
Bright Pixels – 2 Adjacent Green	New panel	n >	All Quadrants	Major Defect
Dark Pixels – Random	New panel	n >	All Quadrants	Minor Defect
Dark Pixels 2 Adjacent	New panel	n >	All Quadrants	Minor Defect
Total Bright and Dark Pixels	New panel	n >	All Quadrants	Major Defect
Distance between Dark Pixels	New panel	< 5mm, n > > 5 mm, n >		Minor Defect
Bright Pixel (Green sub-pixel)	Post reliability stress test	Dia > 0.60, n > 0.30 < Dia ≤ 0.60, n > 0.10 < Dia ≤ 0.30, n >		Major Defect
Distance between bright pixel defects:	Post reliability stress test	< 15 mm n > > 15 mm n >		Major Defect
Dark Pixel	Post reliability stress test	Dia > 0.60, n > 0.30 < Dia ≤ 0.60, n > 0.10 < Dia ≤ 0.30, n >		Minor Defect
Distance between Dark Pixels	Post reliability stress test	< 5 mm, n > > 5 mm, n >		Minor Defect
Bright adjacent pixels	Post reliability stress test	n >		Major Defect
Dark adjacent pixels	Post reliability stress test	n >		Minor Defect
Etch / TFT	New panel or post reliability stress test	Not Allowed	All Quadrants	Major Defect
Light leak	New panel or post reliability stress test	Not Allowed		Major Defect
Static Pooling/ Ripple	New panel or post reliability stress test	None allowed	All Quadrants	Major Defect
Dynamic Pooling/Ripple < 2 sec after cover movement stops No pooling/ripple during system operation	New panel or post reliability stress test	n >	All Quadrants	Major Defect
Total number of all Major and Minor Defects	New panel or post reliability stress test	n >	All Quadrants	All Defects

## 10.0 Panel Reliability:

LCD panel must be qualified thru environmental and reliability testing. This testing may be performed in a notebook system or on stand alone panels. The Limits for testing will be dependent on the system or fixture used in the tests. The reliability tests shown below are typical of those necessary for panel qualification/approval. The sample plan shown below is an example only and is not meant to define a standard test plan. Stand alone LCD panel testing requires that test fixtures be designed and correlated with system test results.

### 10.1 Sample LCD Panel Stand Alone Environmental and Reliability Test Plan

<b><u>Environmental Test</u></b>	<b><u>Test Conditions</u></b>
Operating Life - High Temp.	Temp.= +50°C, Dynamic. 250 Hours
Operating Life - Low Temp.	Temp.= 0°C, Dynamic, 250 Hours
High Temp. Storage Life - Non-Operating	Temp.= +65°C, Non-Operating, 250 Hours
Low Temp. Storage Life	Temp.= -25°C, Non-Operating, 250 Hours
Torsion Test	Panel Twisted to defined limits
High Temp & High Humidity Operating Life	Temp.= +40°C, Dynamic, Humidity 95% ( Non-Condensing), 250 Hours
RCF (Repetitive Compressive Force)	20mm, 80 durometer plunger, 5000 cycles
Shock - Non-Operating	220g's, 2.0 ms, Half Sine Wave ± 3 Axis ( +X, -X, +Y, -Y, +Z, -Z) 3 Shocks per Direction
Vibration - Non-Operating	1.5 Grms, 30 min/side, PSD Spectrum Break Points, 26 Hz G2/Hz=0.316, 50 Hz G2/Hz=0.007, 222 Hz G2/Hz=0.0018, 500Hz G2/Hz=0.0001
Temp. Cycle - Operating	0°C to+40°C, Ramp ≤20°C/min, Duration at Temp. = 30min, Test Cycles = 160
Temp. Cycle - Non-Operating	-25°C to +65°C, Ramp ≤20°C/min, Duration at Temp. = 30min, Test Cycles = 160