TOSHIBA Field Effect Transistor Silicon N-Channel MOS Type (U-MOSⅥ-H)

TPC8051-H

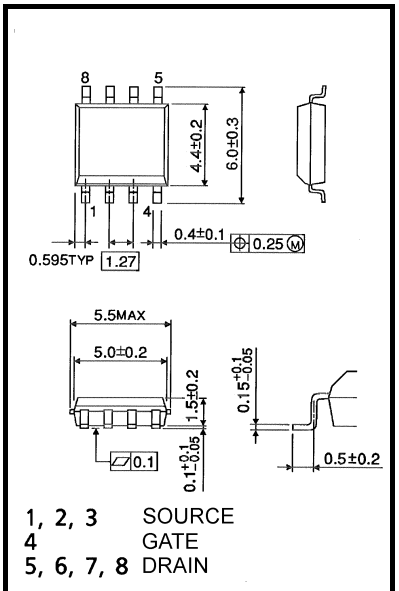
Switching Regulator Applications

Motor Drive Applications

DC-DC Converter Applications

- Small footprint due to a small and thin package
- High-speed switching
- Small gate charge: Q_{SW} = 16 nC (typ.)
- Low drain-source ON-resistance:
  $R_{DS\ (ON)}$ = 6.3 mΩ (typ.)
- High forward transfer admittance: $|Y_{fs}|$ = 45 S (typ.)
- Low leakage current: I_{DSS} = 10 μA (max) (V_{DS} = 80 V)
- Enhancement mode: V_{th} = 1.3 to 2.3 V (V_{DS} = 10 V, I_D = 1.0 mA)

Unit: mm



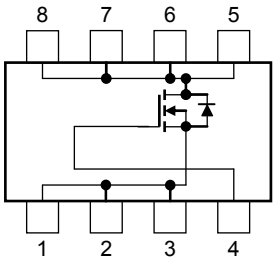
JEDEC	―
JEITA	―
TOSHIBA	2-6J1B

Weight: 0.085g (typ.)

Absolute Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	80	V
Drain-gate voltage (R_{GS} = 20 kΩ)		V_{DGR}	80	V
Gate-source voltage		V_{GSS}	±20	V
Drain current	DC (Note 1)	I_D	13	A
	Pulsed (Note 1)	I_{DP}	52	
Drain power dissipation (t = 10 s) (Note 2a)		P_D	1.9	W
Drain power dissipation (t = 10 s) (Note 2b)		P_D	1.0	W
Single-pulse avalanche energy (Note 3)		E_{AS}	110	mJ
Avalanche current		I_{AR}	13	A
Repetitive avalanche energy (Tc=25°C) (Note 4)		E_{AR}	0.06	mJ
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55 to 150	°C

Circuit Configuration



Note: For Notes 1 to 4, refer to the next page.

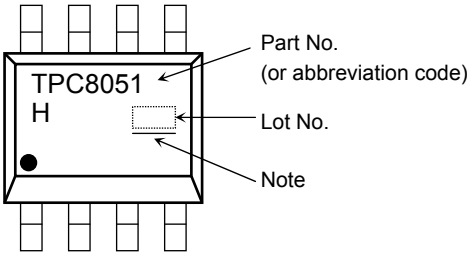
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

This transistor is an electrostatic-sensitive device. Handle with care.

Thermal Characteristics

Characteristic	Symbol	Max	Unit
Thermal resistance, channel to ambient (t = 10 s) (Note 2a)	$R_{th\ (ch\text{-}a)}$	65.8	°C/W
Thermal resistance, channel to ambient (t = 10 s) (Note 2b)	$R_{th\ (ch\text{-}a)}$	125	°C/W

Marking (Note 5)

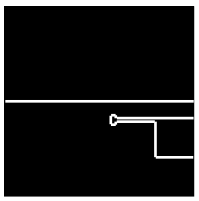


Note : A line under a Lot No. identifies the indication of product Labels
[[G]]/RoHS COMPATIBLE or [[G]]/RoHS [[Pb]]

Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. The RoHS is Directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

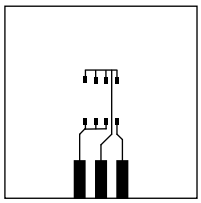
Note 1: Ensure that the channel temperature does not exceed 150°C.

Note 2: (a) Device mounted on a glass-epoxy board (a) (b) Device mounted on a glass-epoxy board (b)



FR-4
25.4 × 25.4 × 0.8
(Unit: mm)

(a)



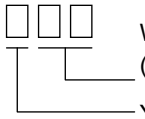
FR-4
25.4 × 25.4 × 0.8
(Unit: mm)

(b)

Note 3: V_{DD} = 24 V, T_{ch} = 25°C (initial), L = 1 mH, R_G = 25 Ω, I_{AR} = 13 A

Note 4: Repetitive rating: pulse width limited by maximum channel temperature

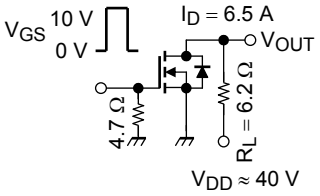
Note 5: * Weekly code: (Three digits)



Week of manufacture
(01 for the first week of the year, continuing up to 52 or 53)

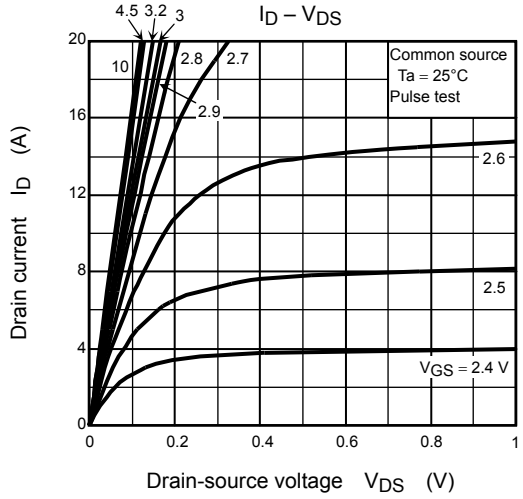
Year of manufacture
(The last digit of the year)

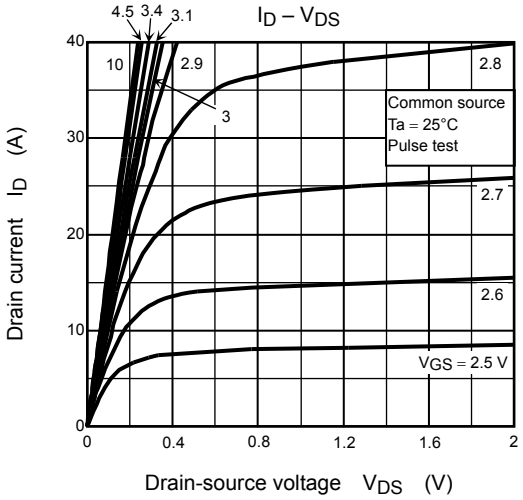
Electrical Characteristics (Ta = 25°C)

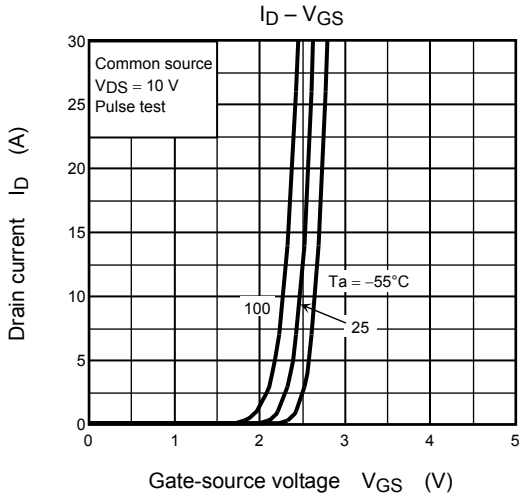
Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V	—	—	±100	nA
Drain cutoff current		I_{DSS}	V_{DS} = 80 V, V_{GS} = 0 V	—	—	10	μA
Drain-source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 10 mA, V_{GS} = 0 V	80	—	—	V
		$V_{(BR)\ DSX}$	I_D = 10 mA, V_{GS} = −20 V	60	—	—	
Gate threshold voltage		V_{th}	V_{DS} = 10 V, I_D = 1.0 mA	1.3	—	2.3	V
Drain-source ON-resistance		$R_{DS\ (ON)}$	V_{GS} = 4.5 V, I_D = 6.5 A	—	6.7	10.1	mΩ
			V_{GS} = 10 V, I_D = 6.5 A	—	6.3	9.7	
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 10 V, I_D = 6.5 A	22.5	45	—	S
Input capacitance		C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	—	5800	7540	pF
Reverse transfer capacitance		C_{rss}		—	150	210	
Output capacitance		C_{oss}		—	520	—	
Gate resistance		rg	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	—	1.0	1.5	Ω
Switching time	Rise time	t_r	 Duty ≤ 1%, t_w = 10 μs	—	3.4	—	ns
	Turn-on time	t_{on}		—	14	—	
	Fall time	t_f		—	6.7	—	
	Turn-off time	t_{off}		—	67	—	
Total gate charge (gate-source plus gate-drain)		Q_g	V_{DD} ≈ 64 V, V_{GS} = 10 V, I_D = 13 A	—	85	—	nC
			V_{DD} ≈ 64 V, V_{GS} = 5 V, I_D = 13 A	—	43	—	
Gate-source charge 1		Q_{gs1}	V_{DD} ≈ 64 V, V_{GS} = 10 V, I_D = 13 A	—	14	—	
Gate-drain (“Miller”) charge		Q_{gd}		—	10	—	
Gate switch charge		Q_{SW}		—	16	—	

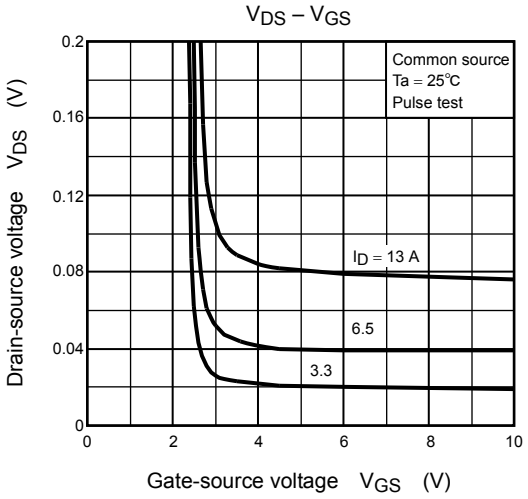
Source-Drain Ratings and Characteristics (Ta = 25°C)

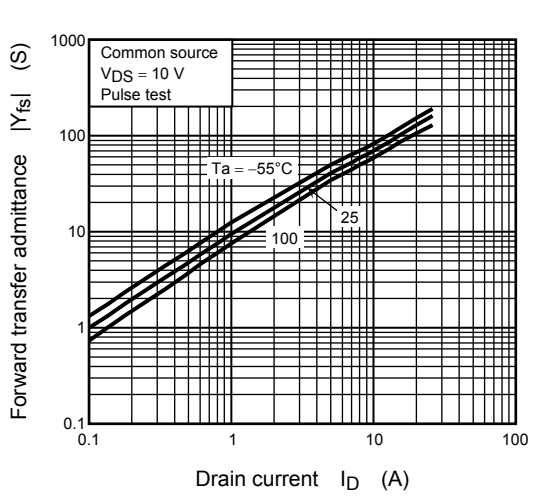
Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Peak forward current	Pulse (Note 1)	I_{FP}	—	—	—	52	A
Forward voltage (diode)		V_{DSF}	I_{DR} = 13 A, V_{GS} = 0 V	—	—	−1.2	V

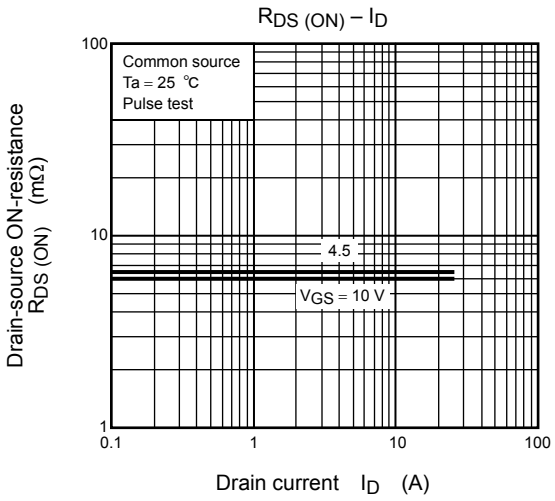

$I_D - V_{DS}$
Common source
Ta = 25°C
Pulse test
4.5
3.2
3
10
2.8
2.7
2.9
2.6
2.5
V_{GS} = 2.4 V
Drain current I_D (A)
Drain-source voltage V_{DS} (V)


$I_D - V_{DS}$
Common source
Ta = 25°C
Pulse test
4.5
3.4
3.1
10
2.9
3
2.8
2.7
2.6
V_{GS} = 2.5 V
Drain current I_D (A)
Drain-source voltage V_{DS} (V)

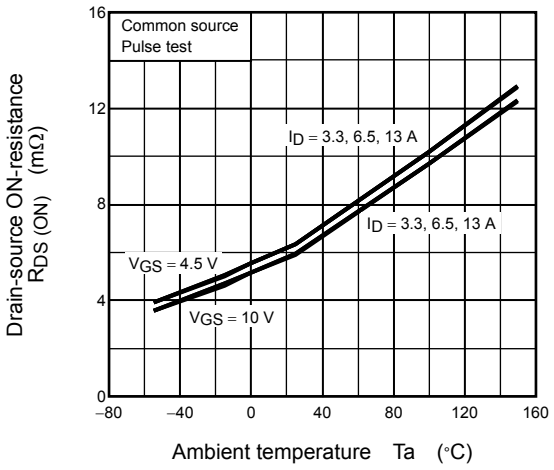

$I_D - V_{GS}$
Common source
V_{DS} = 10 V
Pulse test
Ta = −55°C
100
25
Drain current I_D (A)
Gate-source voltage V_{GS} (V)


$V_{DS} - V_{GS}$
Common source
Ta = 25°C
Pulse test
I_D = 13 A
6.5
3.3
Drain-source voltage V_{DS} (V)
Gate-source voltage V_{GS} (V)

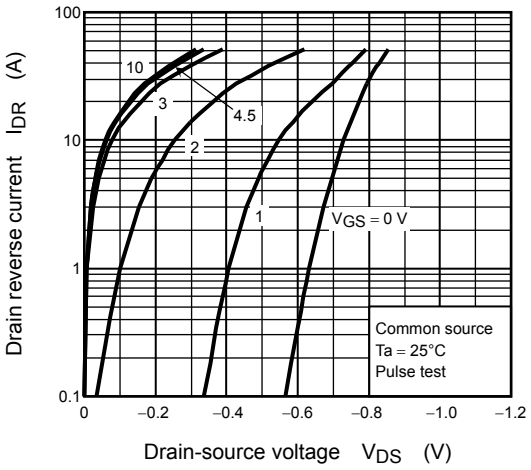

Common source
V_{DS} = 10 V
Pulse test
Ta = −55°C
25
100
Forward transfer admittance $|Y_{fs}|$ (S)
Drain current I_D (A)


$R_{DS\ (ON)} - I_D$
Common source
Ta = 25 °C
Pulse test
4.5
V_{GS} = 10 V
Drain-source ON-resistance $R_{DS\ (ON)}$ (mΩ)
Drain current I_D (A)

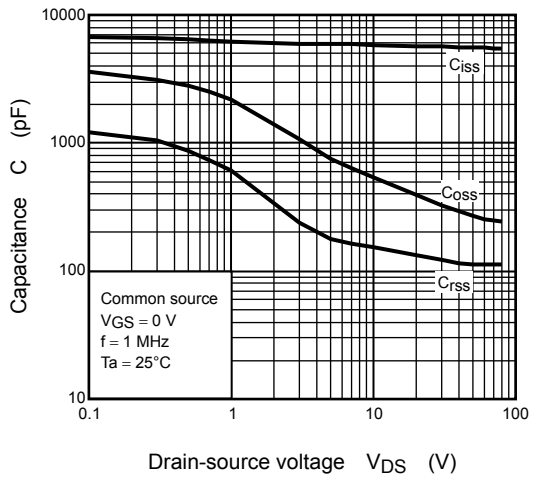
$R_{DS\ (ON)}$ – Ta



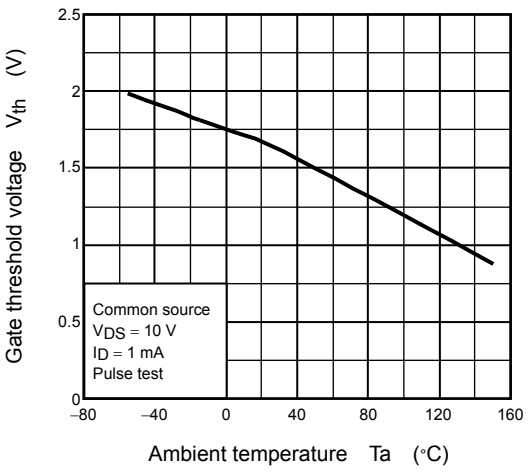
I_{DR} – V_{DS}



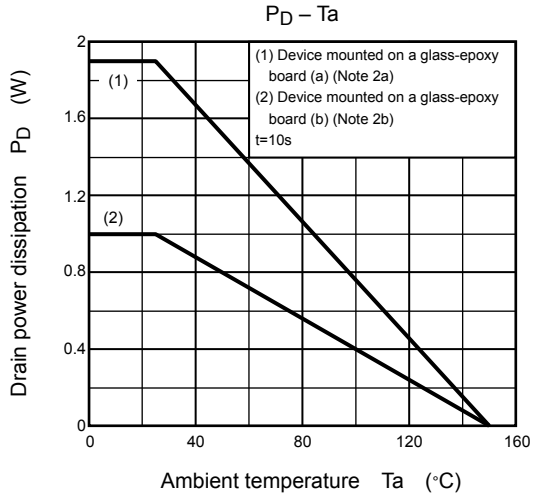
Capacitance – V_{DS}



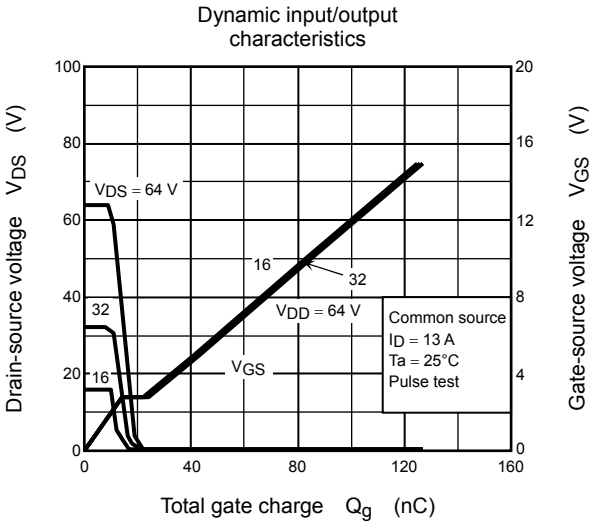
V_{th} – Ta

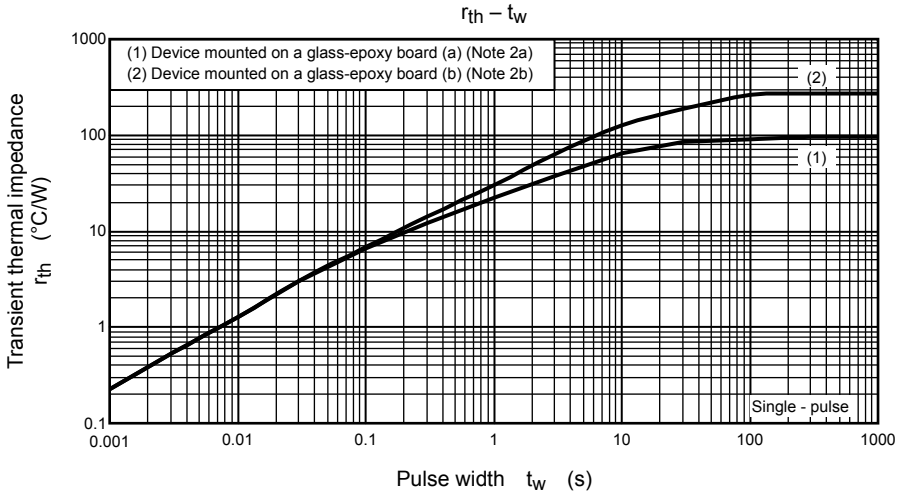


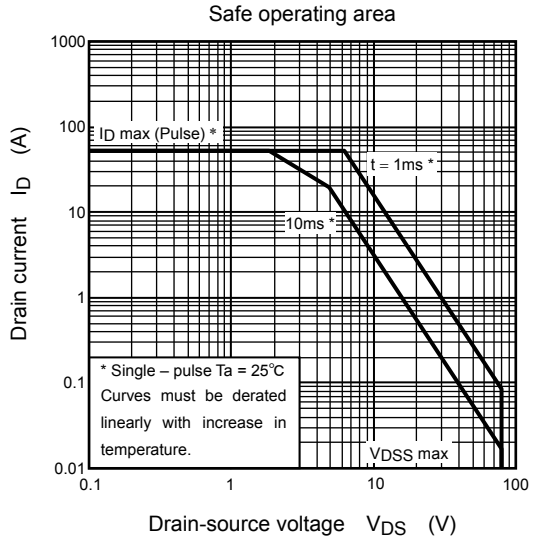
P_D – Ta



Dynamic input/output characteristics




$r_{th} - t_w$
(1) Device mounted on a glass-epoxy board (a) (Note 2a)
(2) Device mounted on a glass-epoxy board (b) (Note 2b)
(2)
(1)
Single - pulse
Transient thermal impedance r_{th} (°C/W)
1000
100
10
1
0.1
0.001
0.01
0.1
1
10
100
1000
Pulse width t_w (s)


Safe operating area
I_D max (Pulse) *
t = 1ms *
10ms *
* Single – pulse Ta = 25°C
Curves must be derated linearly with increase in temperature.
V_{DSS} max
Drain current I_D (A)
1000
100
10
1
0.1
0.01
0.1
1
10
100
Drain-source voltage V_{DS} (V)

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