PFS7323-7329
HiperPFS-2™ Family

High Power PFC Controller with Integrated High-Voltage MOSFET and Qspeed™ Diode

Key Benefits

- Highly integrated for smallest boost PFC form factor
  - Integrated controller and MOSFET in all package options
  - Ultra-low reverse recovery loss diode (Qspeed) included in extended eSIP™ package option
  - Lossless internal current sense reduces component count and system losses
  - EN61000-3-2 Class C and D compliant
- Packaging optimized for high volume production
  - Exposed pad connected to GROUND pin (CoolPAD)
  - Eliminates insulating pad/heat-spreader
- Enhanced features
  - Programmable power good (PG) signal
  - User selectable power limit: Enables device swapping in a given design to optimize efficiency/cost
  - Integrated non-linear amplifier for fast output OV and UV protection
- High efficiency and power factor across load range
  - >95% efficiency from 10% load to full load
  - <200 mW no-load consumption at 230 VAC in remote off-state
  - Light load PF >0.9 at 20% load on optimized designs >200 W
  - PF >0.95 at 50% load
  - Enables 80+ Platinum designs
- Frequency adjusted over line voltage and each line cycle
  - Spread-spectrum across >60 kHz window simplifies EMI filtering requirements
  - Lower boost inductance
- Provides up to 425 W peak output power
  - >425 W peak power in power limit voltage regulation mode

Output Power Table

eSIP-16 Package		
Product	**Maximum Continuous Output Power Rating at 90 VAC (in Full Mode)**	**Peak Output Power Rating**
		Full Mode (R = 24.9 kΩ)
PFS7323L	110 W	120 W
PFS7324L	130 W	150 W
PFS7325L	185 W	205 W
PFS7326H	230 W	260 W
PFS7327H	290 W	320 W
PFS7328H	350 W	385 W
PFS7329H	380 W	425 W

Table 1. Output Power Table (See Table 2 on page 11 for Maximum Continuous Output Power Ratings.)

- Protection features include: UV, OV, OTP, brown-in/out, cycle-by-cycle current limit and power limiting for overload protection
- Halogen free and RoHS compliant

Applications

- PC
- Printer
- LCD TV
- Video game consoles
- High-power adaptors
- High-power LED lighting
- Industrial and appliance
- Generic PFC converters

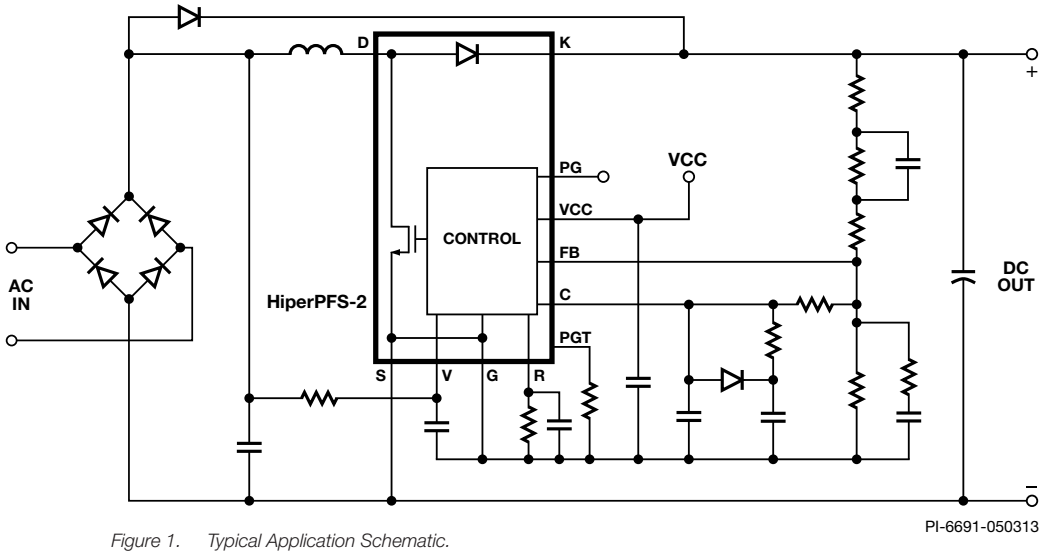

Figure 1. Typical Application Schematic.

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Description

The HiperPFS-2 device family members reach a very high level of integration including a continuous conduction mode (CCM) boost PFC controller, gate driver, ultra-low reverse recovery (Qspeed) diode (eeSIP™ package options) and high-voltage power MOSFET in a single, low-profile CoolPAD (GROUND pin connected) power package that is able to provide near unity input power factor. The HiperPFS-2 devices eliminate the PFC converter's need for external current sense resistors, the power loss associated with those components, and leverages an innovative control technique that adjusts the switching frequency over output load, input line voltage, and even input line cycle. This control technique is designed to maximize efficiency over the entire load range of the converter, particularly at light loads. Additionally, this control technique significantly minimizes the EMI filtering requirements due to its wide bandwidth spread spectrum effect. The HiperPFS-2 also features an integrated non-linear amplifier for enhanced load transient response, a user programmable power good (PG) signal as well as user selectable power limit functionality. HiperPFS-2 includes Power Integrations' standard set of comprehensive protection features, such as integrated soft-start, UV, OV, brown-in/out, and hysteretic thermal shutdown. HiperPFS-2 also provides cycle-by-cycle current limit for the power MOSFET, power limiting of the output for overload protection, and pin-to-pin short-circuit protection.

HiperPFS-2's innovative variable frequency continuous conduction mode of operation (VF-CCM) minimizes switching losses by maintaining a low average switching frequency, while also varying the switching frequency in order to suppress EMI, the traditional challenge with continuous conduction mode solutions. Systems using HiperPFS-2 typically reduce the total X and Y capacitance requirements of the converter, the inductance of both the boost choke and EMI noise suppression chokes, reducing overall system size and cost. Additionally, compared with designs that use discrete MOSFETs and controllers, HiperPFS-2 devices dramatically reduce component count and board footprint while simplifying system design and enhancing reliability. The innovative variable frequency, continuous conduction mode controller enables the HiperPFS-2 to realize all of the benefits of continuous conduction mode operation while leveraging low-cost, small, simple EMI filters.

Many regions mandate high power factor for many electronic products with high power requirements. These rules are combined with numerous application-specific standards that require high power supply efficiency across the entire load range, from full load to as low as 10% load. High efficiency at light load is a challenge for traditional PFC approaches in which fixed MOSFET switching frequencies cause fixed switching losses on each cycle, even at light loads. Besides featuring relatively flat efficiency across the load range, HiperPFS-2 also enables higher power factor at light loads. HiperPFS-2 simplifies compliance with new and emerging energy-efficiency standards over a broad market space in applications such as PCs, LCD TVs, notebooks, appliances, pumps, motors, fans, printers, and LED lighting.

HiperPFS-2 advanced power packaging technology and high efficiency simplifies the complexity of mounting the package and thermal management, while providing very high power capabilities in a single compact package; these devices are suitable for PFC applications from 75 W to 425 W.

Product Highlights

Protected Power Factor Correction Solution

- Incorporates high-voltage power MOSFET, ultra-low reverse recovery loss Qspeed diode, controller, and gate driver
- EN61000-3-2 Class D and Class C compliance
- Integrated protection features reduce external component count
  - Accurate built-in brown-in/out protection
  - Accurate built-in undervoltage (UV) protection
  - Accurate built-in overvoltage (OV) protection
  - Hysteretic thermal shutdown (OTP)
  - Internal power limiting function for overload protection
  - Cycle-by-cycle power switch current limit
  - Internal non-linear amplifier for enhanced load transient response
- No external current sense required
  - Provides 'lossless' internal sensing via sense-FET
  - Reduces component count and system losses
  - Minimizes high current gate drive loop area
- Minimizes output overshoot and stresses during start-up
  - Integrated power limit and frequency soft-start
- Improved dynamic response
  - Input line feed-forward gain adjustment for constant loop gain across entire input voltage range
- Eliminates up to 40 discrete components for higher reliability and lower cost

Intelligent Solution for High Efficiency and Low EMI

- Continuous conduction mode PFC uses novel constant volt/amp-second control engine
  - High efficiency across load
  - High power factor across load
  - Low cost EMI filter
- Frequency sliding technique for light load efficiency improvements
  - >95% efficiency from 10% load to full load at nominal input voltages
- Variable switching frequency to simplify EMI filter design
  - Varies over line input voltage to maximize efficiency and minimize EMI filter requirements
  - Varies with input line cycle voltage by >60 kHz to maximize spread spectrum effect

Advanced Package for High Power Applications

- Up to 425 W peak output power capability in a highly compact package
- Simple adhesive or clip mounting to heat sink
  - No insulation pad required and can be directly connected to heat sink
- Staggered pin arrangement for simple routing of board traces and high-voltage creepage requirements
- Single package solution for PFC converter reduces assembly costs and layout size

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Pin Functional Description

VOLTAGE MONITOR (V) Pin:
The VOLTAGE MONITOR pin is tied to the rectified high-voltage DC rail through a large resistor (4 MΩ ±1%) to minimize power dissipation and standby power consumption. Modifying this resistor value affects peak power limit, brown-in/out thresholds and will degrade input current quality (reduce power factor and increase THD). A small ceramic capacitor (22 nF) is required from the VOLTAGE MONITOR pin to SIGNAL GROUND pin to bypass any switching noise present on the rectified DC bus. This pin also features brown-in/out detection thresholds.

REFERENCE (R) Pin:
This pin is connected to an external precision resistor and is used for an internal current reference source in the controller. The external resistor is tied between the REFERENCE and SIGNAL GROUND pins. The REFERENCE pin only has two valid resistor values to select 'Full' (24.9 kΩ ±1%) and 'Efficiency' (49.9 kΩ ±1%) power modes. A precision resistor with the values specified above must be selected since this sets the internal current reference for the controller. Other values beyond what is specified may adversely effect the operation of the device. A bypass capacitor is also recommended across the REFERENCE pin resistor to the SIGNAL GROUND pin. For 'Full' power mode (24.9 kΩ) a capacitor value of 470 pf and 1 nF for the 'Efficiency' mode with 49.9 kΩ.

SIGNAL GROUND (G) Pin:
Discrete components used in the feedback circuit, including loop compensation, decoupling capacitors for the supply (VCC) and line-sense (V) must be referenced to the SIGNAL GROUND pin. The SIGNAL GROUND pin is also connected to the tab of the device. **The SIGNAL GROUND pin must not be tied to the SOURCE pin**.

COMPENSATION (C) Pin:
This pin is used for loop compensation and voltage feedback. The COMPENSATION pin is a high input-impedance reference terminal that connects to the main voltage regulation feedback resistor divider network. This pin also connects to the loop compensation components comprising of a series RC network. A 22 nF capacitor is also required between the COMPENSATION and SIGNAL GROUND pins; this capacitor must be placed very close to the device on the PCB to bypass any switching noise.

FEEDBACK (FB) Pin:
This pin is connected to the main voltage regulation feedback resistor divider network and is used for fast over and under-voltage protection. This pin also detects the presence of the main voltage divider network at start-up.

POWER GOOD THRESHOLD (PGT) Pin:
This pin is used to program the output voltage threshold where the PG signal becomes 'high-impedance' representing the PFC stage falling out of regulation. The low threshold for the PG signal is programmed with a resistor between the POWER GOOD THRESHOLD and SIGNAL GROUND pins.

POWER GOOD (PG) Pin:
This pin is an open-drain connection that indicates that the output voltage is in regulation. At start-up, once the FEEDBACK pin voltage has risen to ~95% of the set output voltage, the POWER GOOD pin is pulled low. After start-up the output voltage threshold at which the PG signal becomes high-impedance depends on the threshold programmed by the POWER GOOD THRESHOLD pin resistor.

BIAS POWER (VCC) Pin:
This is a 10.2-13 VDC bias supply used to power the IC. The bias voltage must be externally clamped to prevent the BIAS POWER pin from exceeding 15 VDC.

SOURCE (S) Pin:
This pin is the source connection of the power switch.

DRAIN (D) Pin:
This is the drain connection of the internal power switch.

BOOST DIODE CATHODE (K) Pin: (eSIP-16 package only)
This is the cathode connection of the internal Qspeed Diode.

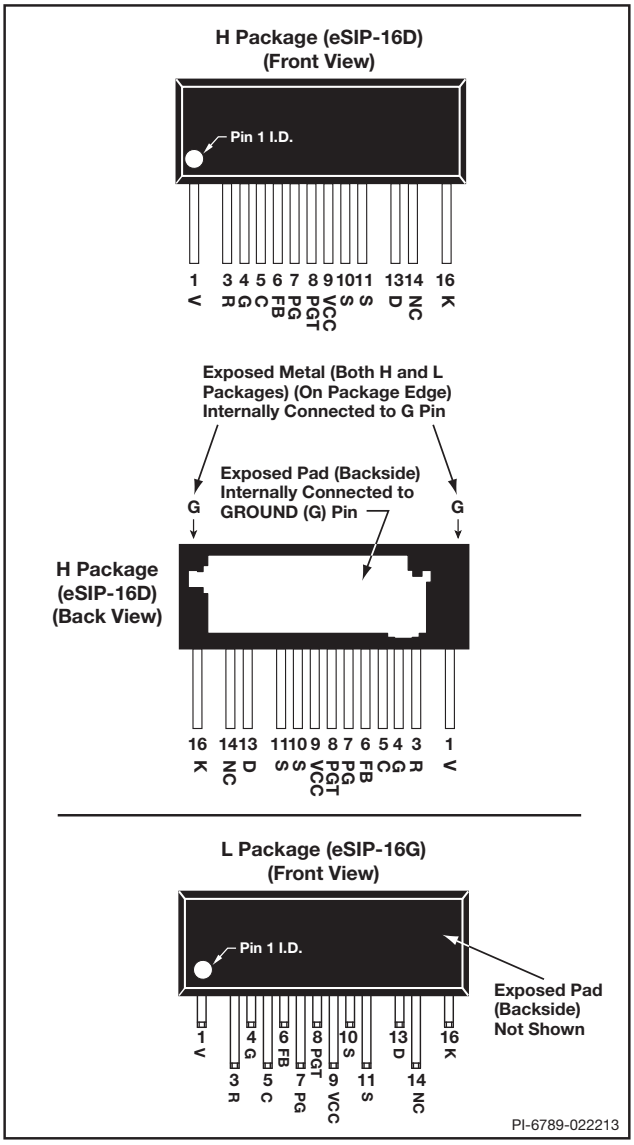

Figure 2. Pin Configuration.

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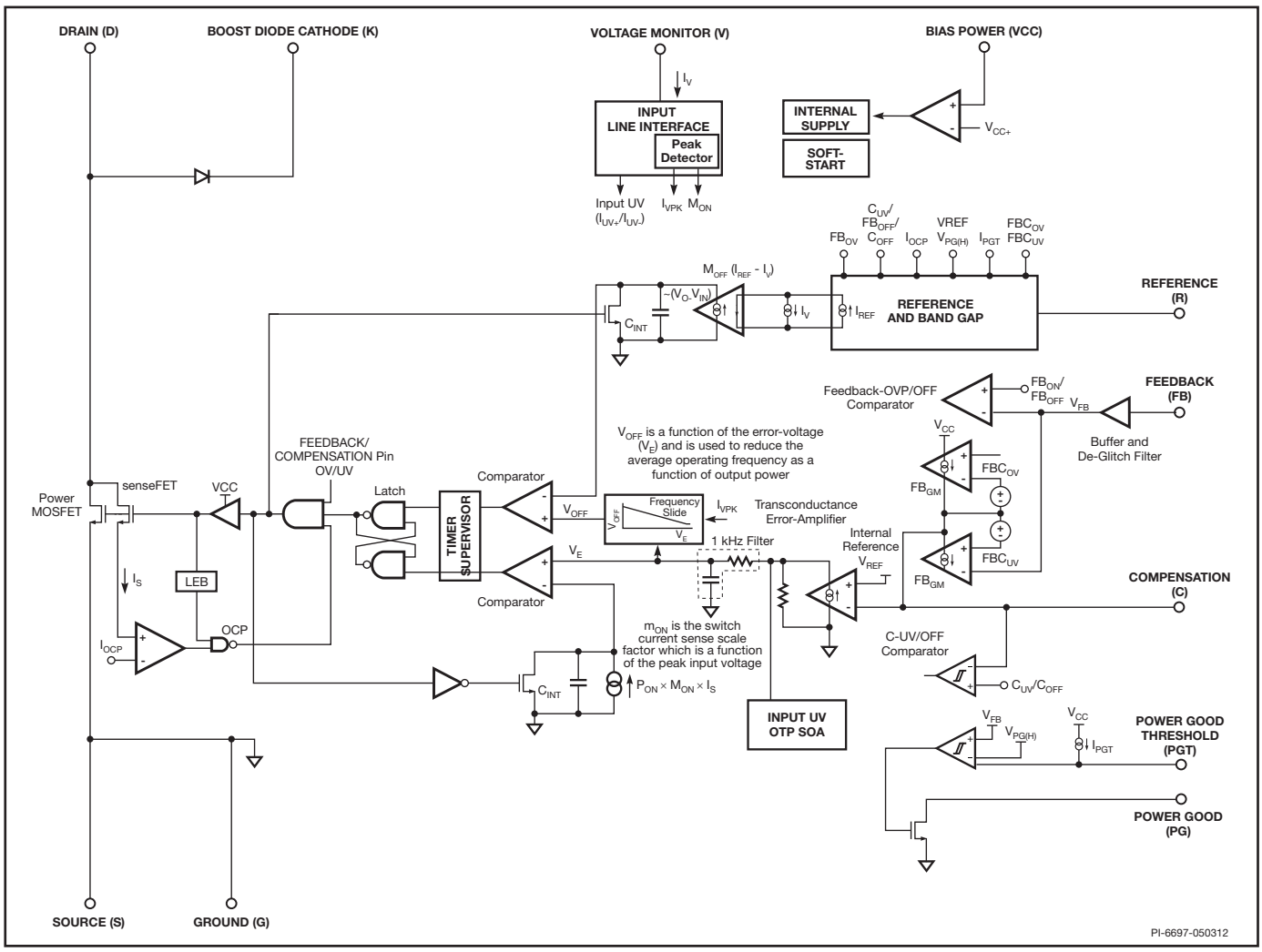

Figure 3. Functional Block Diagram.

Functional Description

The HiperPFS-2 is a variable switching frequency boost PFC solution. More specifically, it employs a constant amp-second on-time and constant volt-second off-time control algorithm. This algorithm is used to regulate the output voltage and shape the input current to comply with regulatory harmonic current limits (high power factor). Integrating the switch current and controlling it to have a constant amp-sec product over the on-time of the switch allows the average input current to follow the input voltage. Integrating the difference between the output and input voltage maintains a constant volt-second balance dictated by the electro-magnetic properties of the boost inductor and thus regulates the output voltage and power.

More specifically, the control technique sets constant volt-seconds for the off-time (t_{OFF}). The off-time is controlled such that:

$$(V_O - V_{IN}) \times t_{OFF} = K_1 \qquad (1)$$

Since the volt-seconds during the on-time must equal the volt-seconds during the off-time, to maintain flux equilibrium in the PFC choke, the on-time (t_{ON}) is controlled such that:

$$V_{IN} \times t_{ON} = K_1 \qquad (2)$$

The controller also sets a constant value of charge during each on-cycle of the power MOSFET. The charge per cycle is varied gradually over many switching cycles in response to load changes so it can be regarded as substantially constant for a half line cycle. With this constant charge (or amp-second) control, the following relationship is therefore also true:

$$I_{IN} \times t_{ON} = K_2 \qquad (3)$$

Substituting t_{ON} from (2) into (3) gives:

$$I_{IN} = V_{IN} \times \frac{K_2}{K_1} \qquad (4)$$

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The relationship of (4) demonstrates that by controlling a constant amp-second on-time and constant volt-second off-time, the input current I_{IN} is proportional to the input voltage V_{IN}, therefore providing the fundamental requirement of power factor correction.

This control produces a continuous mode power switch current waveform that varies both in frequency and peak current value across a line half-cycle to produce an input current proportional to the input voltage.

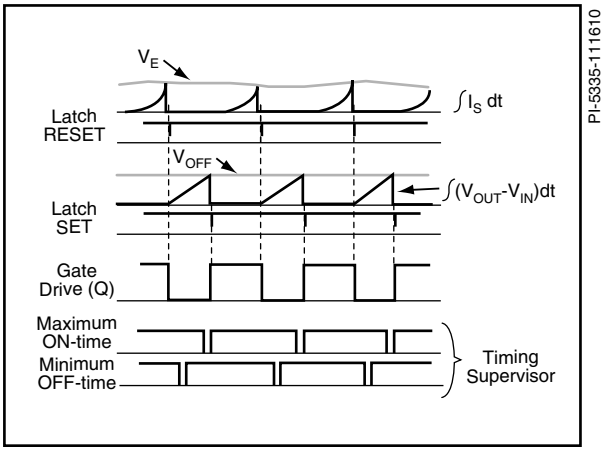

Figure 4. Idealized Converter Waveforms.

Control Engine

The controller features a low bandwidth error-amplifier which connects its non-inverting terminal to an internal voltage reference of 6 V. The inverting terminal of the error-amplifier is available on the external CONTROL pin which connects to the loop compensation and voltage divider network to regulate the output voltage. The FEEDBACK pin connects directly to the divider network for fast transient load response.

The internal sense-FET switch current is integrated and scaled by the input voltage peak detector current sense gain (M_{ON}) and compared with the error-amplifier signal (V_E) to determine the cycle on-time. Internally the difference between the input and output voltage is derived and the resultant is scaled, integrated, and compared to a voltage reference (V_{OFF}) to determine the cycle off-time. Careful selection of the internal scaling factors produce input current waveforms with very low distortion and high power factor.

Line Feed-Forward Scaling Factor (M_{ON})

The VOLTAGE MONITOR (V) pin current is used internally to derive the peak of the input line voltage which is used to scale the gain of the current sense signal through the M_{ON} variable. This contribution is required to reduce the dynamic range of the control feedback signal as well as maintain a constant loop gain over the operating input line range. This line-sense feed-forward gain adjustment is proportional to the square of the peak rectified AC line voltage and is adjusted as a function of VOLTAGE MONITOR pin current. The line-sense feed-forward gain is also important in providing a switch power limit over the input line range. Besides modifying brown- in/out thresholds, the VOLTAGE MONITOR pin resistor also affects power limit of the device.

This characteristic is optimized to maintain a relatively constant internal error-voltage level at full load from an input line of 100 to 230 VAC input.

Beyond the specified peak power rating of the device, the internal power limit feature will regulate the output voltage below the set regulation threshold as a function of output overload beyond the peak power rating. Figure 5 illustrates the typical regulation characteristic as function of load.

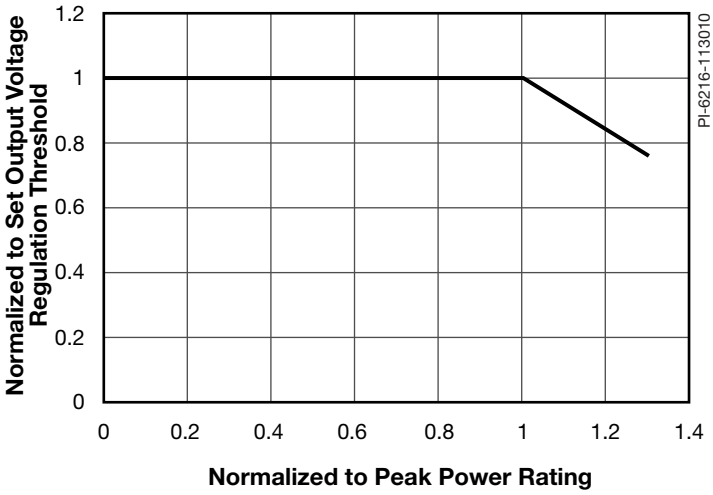

Figure 5. Typical Normalized Output Voltage Characteristics as Function of Normalized Peak Load Rating

Below the brown-in threshold (I_{UV+}) the power limit is reduced when the device is operated in the 'Full' power mode as shown in the figure below.

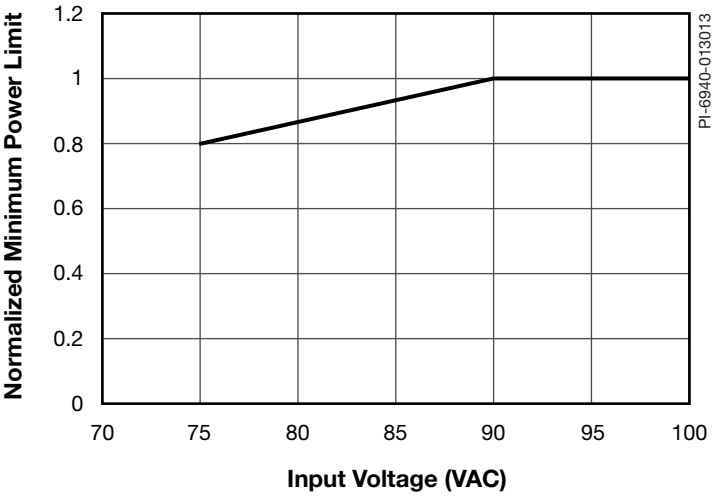

Figure 6. Normalized Minimum Power Limit as Function of Input Voltage.

As the input line voltage is reduced toward the brown-out threshold (I_{UV-}) and if the load exceeds the power limit derating the boost output voltage will drop out of regulation in accordance to Figure 6.

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The minimum rated peak power shown in Table 1 is not derated below the brown-in threshold when the device is operated in the 'Efficiency' mode.

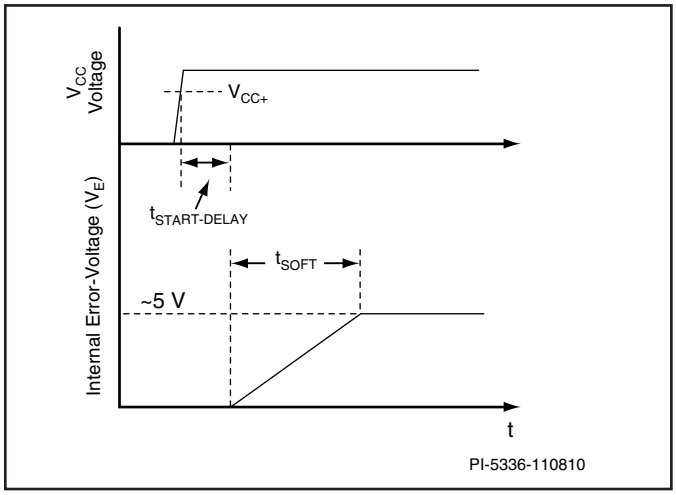

Figure 7. Power Limit Soft-Start Function.

Soft-Start with Pin-to-Pin Short-Circuit Protection

The FEEDBACK pin which is connected to a resistor voltage divider provides a means to overcome the inherently slow feedback loop response. The controller has an integrated non-linear amplifier function to limit the maximum overshoot and undershoot during load transient events.

To reduce switch and output diode current stress at start-up, the HiperPFS slews the internal error-voltage from zero to its steady-state value at start-up. Figure 7 illustrates the relative relationship between the application of V_{CC} and power limit soft-start function through the internal error-voltage. The error-voltage has a controlled slew rate of 0.25 V/ms at start-up, corresponding to the t_{SOFT} time duration for a full scale error voltage of 5 V.

The beginning of soft-start is gated by the V_{CC+}, REFERENCE, CONTROL and FEEDBACK pin voltage thresholds in the sequence described below. Once the applied VCC is above the VCC+ threshold, conditions for REFERENCE, COMPENSATION

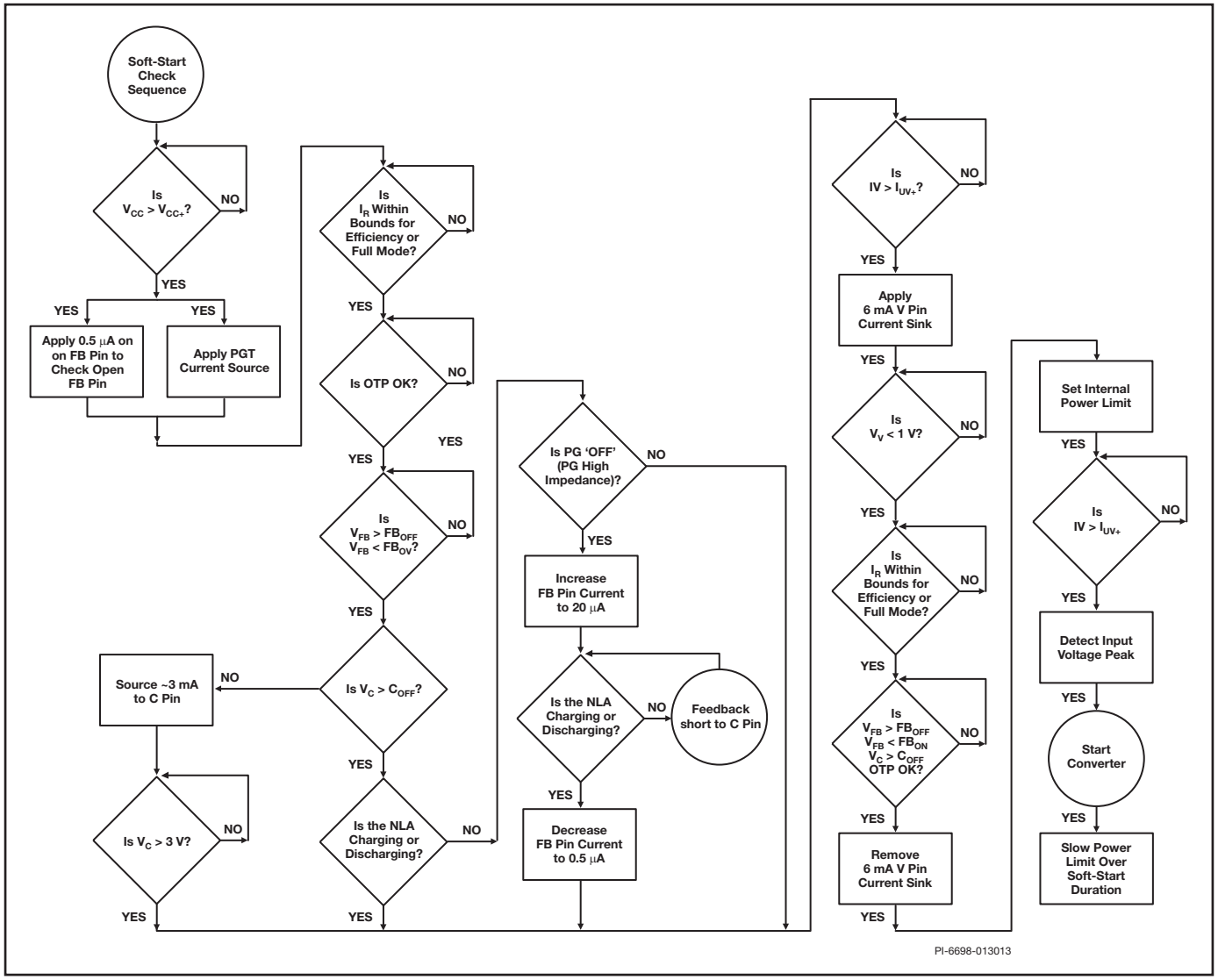

Figure 8. Start-Up Sequence.

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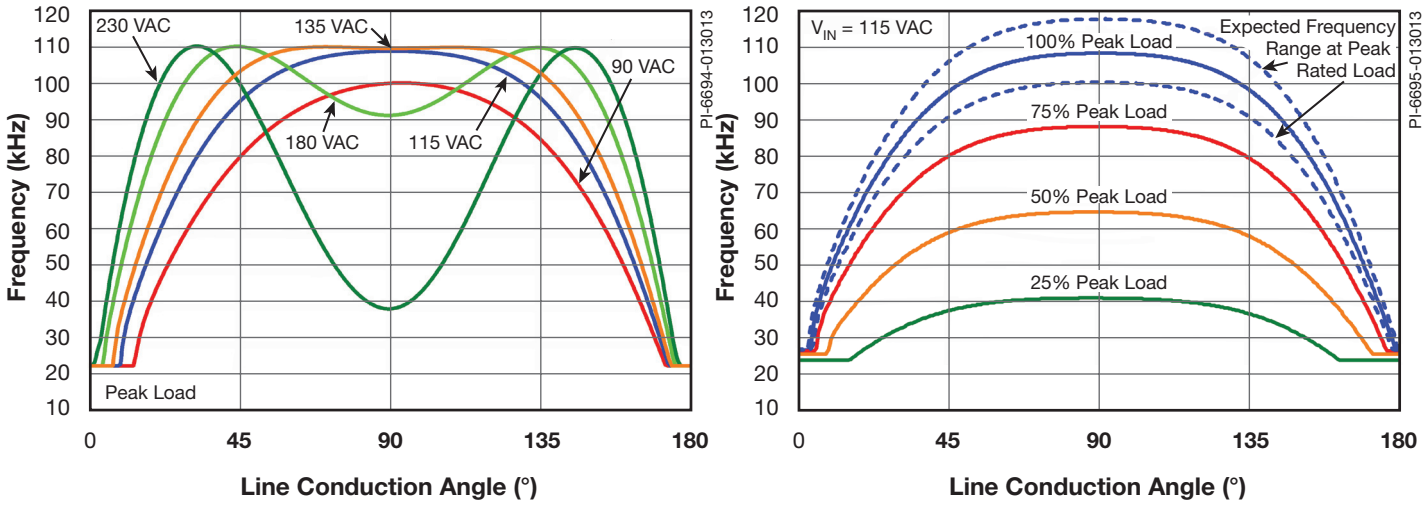

Figure 9. (a) Frequency Variation Over Line Half-Cycle as a Function of Input Voltage (b) Frequency Variation Over Line Half-Cycle as a Function of Load.

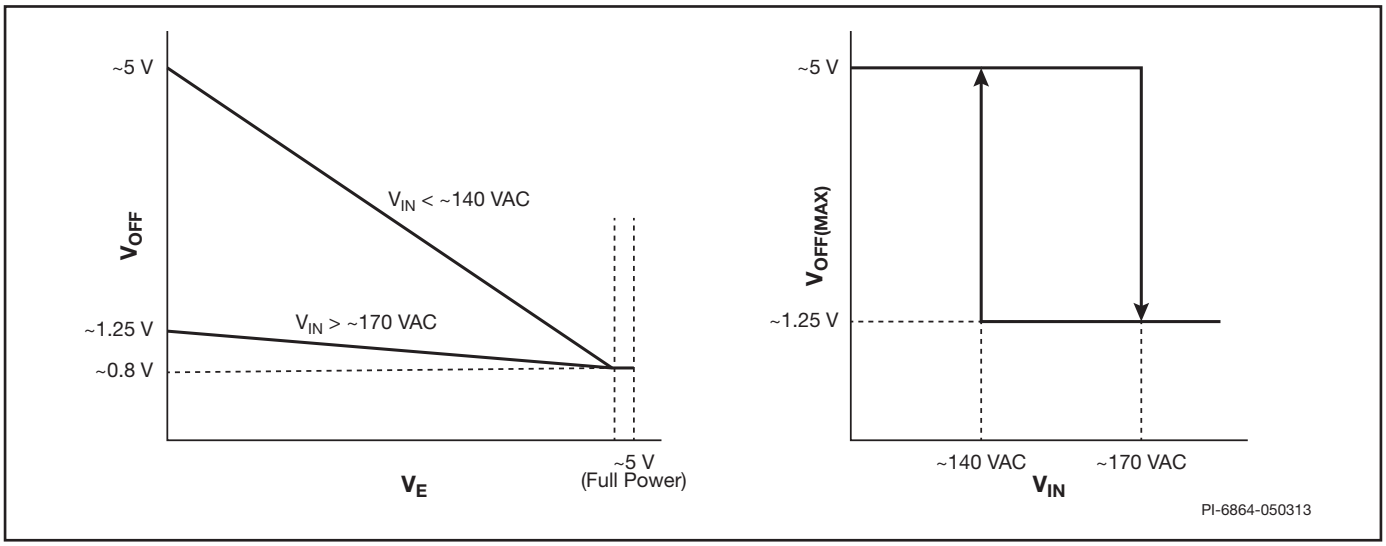

Figure 10. V_{OFF} vs. V_E and V_{OFF} vs. Input Voltage.

and FEEDBACK pins are satisfied and the sensed VOLTAGE MONITOR pin current is above I_{UV+} ,the IC applies a ~6 mA current sink through the VOLTAGE MONITOR pin and checks that the status of the REFERENCE pin voltage is still in a valid range. This checks to ensure that the FEEDBACK and REFERENCE pins are not shorted together. In the event that these pin voltage are shorted or the REFERENCE pin current is no longer in the valid range, VOLTAGE MONITOR pin holds the 6 mA current sink indefinitely until the REFERENCE pin is in the valid range. Figure 8 illustrates this sequence.

Timing Supervisor and Operating Frequency Range

Since the controller is expected to operate with a variable switching frequency over the line frequency half-cycle, typically spanning a range of 24 – 110 kHz, the controller also features a timing supervisor function which monitors and limits the maximum switch on-time and off-time as well as ensures a minimum cycle off-time.

Figure 9a shows the typical half-line frequency profile of the device switching frequency as a function of input voltage at peak load conditions. Figure 9b shows for a given line condition the effect of EcoSmart™ to the switching frequency as a function of load. The switching frequency is not a function of boost choke inductance in CCM (continuous conduction mode) operation.

EcoSmart

The HiperPFS-2 includes an EcoSmart mode wherein the internal error signal (V_E) is used to detect the converter output power. Since the internal error-signal is proportional to the output power, this signal level is used to set the average switching frequency as a function of output power. The off-time integrator control reference (V_{OFF}) is controlled with respect to the internal error-voltage level (output power) to allow the converter to maintain output voltage regulation and relatively flat conversion efficiency between 20% to 100% of rated load

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which is essential to meet many efficiency directives. The degree of frequency slide is also controlled as a function of peak input line voltage, at high input line the maximum off-time voltage reference at zero error-voltage will be approximately 1/4 of the maximum value at low input line conditions.

The lower V_{OFF} slope reduces the average frequency swing for high input line operation.

Burst-Mode for No-Load Power Consumption Reduction
Unlike the original HiperPFS which had the ability to reduce the minimum on-time to zero, the minimum on-time in HiperPFS-2 has a minimum value of 500 ns to enable burst-mode operation at no-load.

Since the minimum on-time is 500 ns, at no-load the output voltage will climb until the device shuts off due to the voltage on the COMPENSATION pin reaching the C_{OV} threshold. The output voltage ripple at no-load to light load will be increased as a result of the burst-mode operation.

A higher minimum on-time and inclusion of the C_{OV} comparator are the main elements in the design to enable this burst-mode operation at no-load. The burst-mode was added to reduce the power stage no-load consumption to below 0.5 W when the boost converter is designed with a ferrite boost choke.

Power Good Signal (PG)
The HiperPFS-2 features a 'power good' (PG) circuit which comprises of an internal comparator that at start-up turns 'on' a switch when the sensed output voltage on the FEEDBACK pin rises to ~95% ($V_{PG(H)}$ threshold) of the set output voltage threshold. During start-up prior to the output voltage reaching $V_{PG(H)}$ the PG signal is in a high-impedance state (internal switch is in 'off' state).

When the AC input voltage is removed or other fault occurs after start-up, the power good signal transitions from 'on' to 'off' state once the sensed output voltage on the FEEDBACK pin falls to a user selected threshold programmed with a resistor on the POWER GOOD THRESHOLD pin. The POWER GOOD THRESHOLD pin has a fixed source current of I_{PGT} and this combined with the power good threshold resistor sets the threshold when the power good signal transitions from the 'on' state to the high-impedance high-state as the PFC output voltage falls out of regulation.

The POWER GOOD THRESHOLD pin has an internal 100 μs de-glitch filter (t_{PG}) to prevent noise events from falsely setting the $V_{PG(L)}$ threshold.

In the event a load fault prevents the boost from achieving regulation (~95% of the set output voltage threshold) the PG function will remain in the high-impedance state and will not annunciate when a output voltage has fallen below the user programmed $V_{PG(L)}$ threshold.

The $V_{PG(L)}$ user programmed threshold is enabled once $V_{PG(H)}$ threshold has been reached.

If the PGT programming resistor is left open, the power good function is disabled and remains in the high-impedance ('off') state, whereas if the POWER GOOD THRESHOLD pin is shorted to the GROUND pin the power good signal will remain in the low ('on') state until the PFC output voltage has fallen to the C_{UV} threshold.

Similar to the condition described above, if the value of the PGT resistor is such that the $V_{PG(L)}$ threshold is greater than the $V_{PG(H)}$ threshold the PG signal will remain in the high-impedance off-state.

Power good function is not valid under the following conditions:

A. VCC is not in a valid range. Below V_{CC-}, the power good function is not valid.
B. REFERENCE pin resistor is in an invalid range. If the REFERENCE pin resistor is not either 24. 9 kΩ for 'Full' or 49.9 kΩ for 'Efficiency' mode, the power good signal is not valid. Power good will go to high-impedance state (internal MOSFET is 'off') at the end of the fast soft-shutdown initiated by the REFERENCE pin resistor fault.
C. The valid programming range of PGT is between 275 V to 360 V. Programming an output voltage below 275 VDC to trigger PG is invalid.

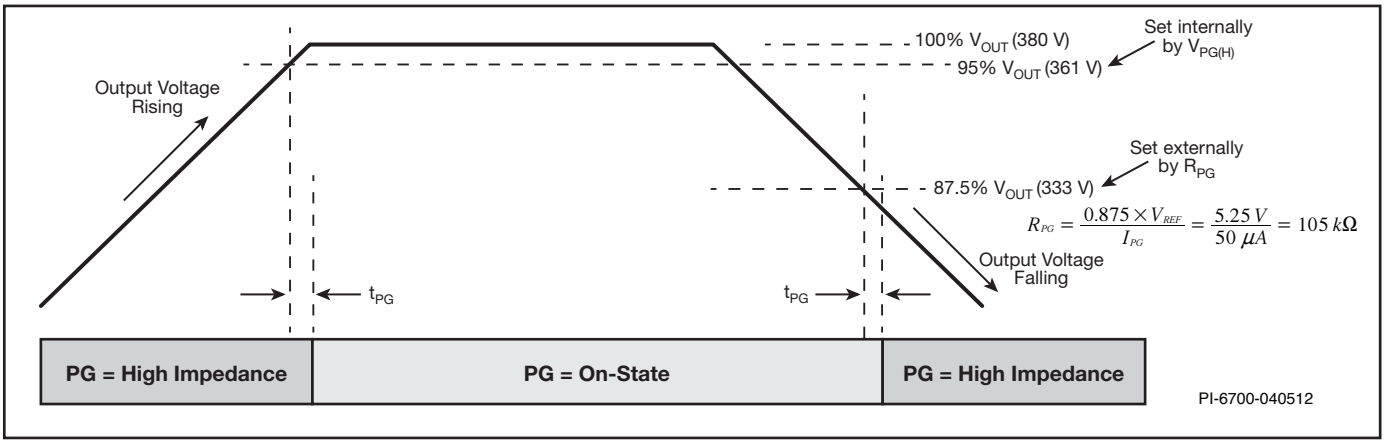

Figure 11. Power Good Function Description.

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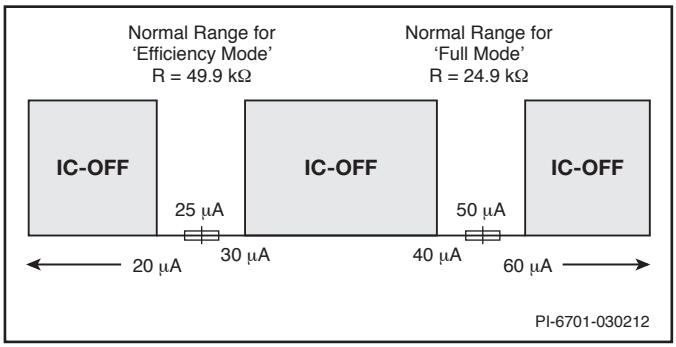

Figure 12. REFERENCE Pin Current Operating Range.

D. Once the start-up sequence check has passed and the converter goes into soft-start and if PGT is shorted to SIGNAL GROUND pin, then the PG signal will toggle to the low state (internal MOSFET is 'on') when the output voltage reaches 85-100% of the set regulation threshold and will remain in this state until the output voltage reaches zero volt or conditions in A, B or C occur.
E. Once the start-up sequence check has passed and the converter goes into soft-start and if PGT is open, then the PG signal will remain in the high-impedance state (internal MOSFET is 'off').

Reference and Selectable Power Limit

Besides the internal current reference source, the precision resistor on the REFERENCE pin also allows user selection between 'full' and 'efficiency' power limit for each device. The efficiency power mode will permit user selection of a larger device for a given output power requirement for increased conversion efficiency.

In 'full' power mode the REFERENCE pin resistor is 24.9 kΩ ±1% and the 'Efficiency' power limit mode is selected with a 49.9 kΩ ±1% resistor.

If the REFERENCE pin is shorted (to GROUND pin) or open circuited the IC will initiate a fast soft-shutdown and disable the power MOSFET and remain disabled until all the conditions for the start-up sequence are satisfied.

The REFERENCE pin resistor value and power mode is latched at start-up.

Protection Modes

VOLTAGE MONITOR (V) Pin Shutdown

The VOLTAGE MONITOR pin features a shutdown protection mode which can be used with the VOLTAGE MONITOR pin resistor or external circuitry to cover system faults. During start-up (1 V < VFB < 5.8 V) in the event the current through the VOLTAGE MONITOR pin exceeds the $I_{V(OFF)}$ threshold for a duration exceeding approximately (1 μs), the IC disables the internal MOSFET for the entire duration that the VOLTAGE MONITOR pin current is above $I_{V(OFF)}$. In normal operation, if the current through the VOLTAGE MONITOR pin exceeds the $I_{V(OFF)}$ threshold for a duration exceeding $t_{V(OFF)}$, the IC will re-initiate the start-up sequence.

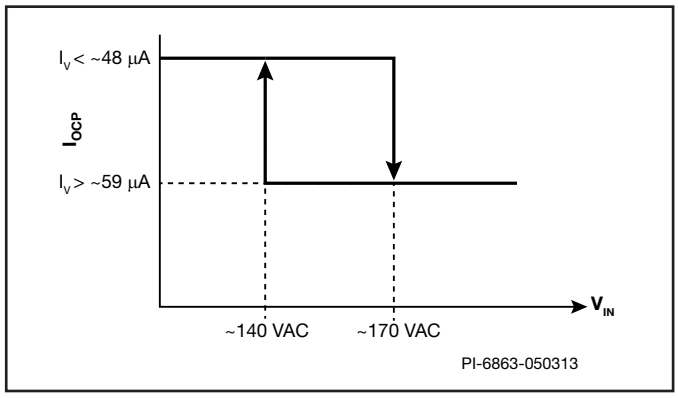

Figure 13. Line Dependent OCP.

Brown-In Protection (I_{UV+})

The VOLTAGE MONITOR pin features an input line undervoltage detection to limit the minimum start-up voltage detected through the VOLTAGE MONITOR pin. This detection threshold will inhibit the device from starting at very low input AC voltage.

Brown-Out Protection (I_{UV-})

The VOLTAGE MONITOR pin features a brown-out protection mode wherein the HiperPFS will turn-off when the VOLTAGE MONITOR pin current is below the Line UV- threshold (I_{UV-}) for a period exceeding the $t_{BROWN-OUT}$ time period. In the event a single half-line cycle is missing (normal operating line frequency is 47 to 63 Hz) the brown-out protection will not be activated. The HiperPFS-2 soft-shutdown in effect gradually reduces the internal error-voltage to zero volts at rate of 1 V/ms to decay the power MOSFET on-time to zero.

At peak power (V_E ~5 V) the shutdown time will be approximately 5 ms. The internal error-voltage is held at 0 V for as long as the input peak voltage is below the brown-in (I_{UV+}) threshold. The internal error-voltage controlled slew to 0 V gradually reduces the switch on-time to zero to deplete energy stored in the boost choke as well as input EMI filter for power-down. Once the error-voltage reaches zero volts the controller is effectively in an off-state (gated by 5 ms timer) and will restart once all the conditions of soft-start are satisfied.

At start-up and during soft-start the brown-out threshold (same as Line UV-) is reduced to $I_{UV(SS)}$ and brown-out timer is also extended to $t_{UV(SS)}$ (soft-start brown-out timer).

Soft-start brown-out threshold ($I_{UV(SS)}$) is reset to I_{UV-} once the internal error-voltage has begun to fall (indicating the converter has reached steady-state output voltage regulation).

The soft-start brown-out timer is reset to the normal brown-out timer once the internal error-voltage has begun to fall (indicating the converter has reached steady-state output voltage regulation) and the VOLTAGE MONITOR pin current exceeds I_{UV-}.

If the VOLTAGE MONITOR pin current is still below the $I_{UV(SS)}$ threshold after the end of the soft-start brown-out timer ($t_{UV(SS)}$), then the converter will fail to start and initiate a soft-shutdown followed by a soft start-up sequence as described in flowchart in Figure 8.

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Temporarily reducing the brown-out threshold prevents false turn-off at high power start-up when voltage drop across the input bridge rectifier and filter stage may cause the rectified input to sag below the brown-out threshold.

Increasing the brown-out timer during soft-start permits a longer time for an in-line AC-side NTC to reduce its resistance and increase the voltage presented to the VOLTAGE MONITOR pin.

In the event the converter does not reach regulation at start-up (overload or power limit condition) C_{UV} protection threshold is not activated and both the $I_{UV(SS)}$ and $t_{UV(SS)}$ are not reset.

It is expected that while the input voltage peak is below the brown-out threshold (I_{UV-}) during a line cycle drop out or line sag event the internal peak detector will force refresh the line feed-forward gain (m_{ON}) to the minimum value at the $t_{REFRESH}$ sample rate.

Similar to the original HiperPFS, the controller latches the OCP threshold in the event of an AC line cycle drop-out when the peak sense is for a high input line condition (V_{IN} > 170 VAC).

Fast Output Voltage Overvoltage Protection (FB_{ov})
This family features a FEEDBACK pin that is connected directly to the output voltage resistor divider network to permit fast feedback information to the controller for fast load transient response.

The COMPENSATION pin which is also connected to the voltage divider network includes a resistor to isolate the slow feedback path and loop compensation network into the controller for steady-state output voltage regulation.

Comparators on the FEEBACK and COMPENSATION pins are used to verify that the pins are not open-circuited and that the main voltage divider voltage at start-up is greater than FB_{OFF} and C_{OFF} in order to complete the start-up fault detect sequence. After start-up the FB_{OFF} and C_{OFF} thresholds remain enabled.

Similarly to the original HiperPFS, this controller includes internal FB_{OV} (FEEDBACK pin overvoltage), C_{OV} (COMPENSATION pin overvoltage) and C_{UV} (COMPENSATION pin undervoltage) protection thresholds that are detected through the FEEDBACK and COMPENSATION pins. Deglitch filters ($t_{FB(OV)}$ and $t_{C(UV)}$) are also used to prevent the controller from falsely triggering this protection mode.

A FB_{OV} event in excess of the $t_{FB(OV)}$ delay will terminate the switch cycle immediately.

The COMPENSATION pin also features an output voltage undervoltage detection threshold to detect an overload or open-loop condition (broken feedback). In the event the falling edge of the voltage on the COMPENSATION pin falls below the C_{UV} threshold, the MOSFET is disabled and the soft-start start-up sequence is initiated.

The COMPENSATION pin undervoltage protection (C_{UV}) mode is disabled during start-up and enabled once the COMPENSATION pin voltage exceeds approximately 5.8 V. The brown-out threshold is also reset from $I_{UV(SS)}$ to I_{UV-} under the same conditions as activation of the C_{UV} threshold.

VCC Undervoltage Protection (UVLO)
The BIAS POWER (VCC) pin has an undervoltage lock-out protection which inhibits the IC from starting unless the applied VCC voltage is above the VCC+ threshold. The IC initiates a soft-start once the VCC pin voltage exceeds the VCC+ threshold. After start-up the IC will continue to operate until the VCC pin voltage has fallen below VCC- level. The absolute maximum voltage of the VCC pin is 15 V which must be externally limited to prevent damage to the IC.

Over-Current Protection
The device includes a cycle-by-cycle over-current-protection (OCP) mode which protects the device in the event of a catastrophic fault. The OCP mode in the HiperPFS-2 is input line dependent as shown in Figure 13. The intention of OCP in this device is strictly protection of the internal power MOSFET and is not intended to protect the converter from output short-circuit or overload fault conditions.

The HiperPFS-2 latches the high input line OCP for a 1/2 line cycle and updates the OCP status after the expiration of a 5 ms block-out timer. This feature has particular benefit for hard-start after an AC line cycle drop where the peak detector may falsely detect a low input line condition even though the input is at high input line.

A leading edge blanking circuit inhibits the current limit comparator for a short time (t_{LEB}) after the power MOSFET is turned on. This leading edge blanking time is set so that current spikes caused by capacitance and rectifier reverse recovery time will not cause premature termination of the MOSFET conduction.

Safe Operating Area (SOA) Mode
Since the cycle-by-cycle OCP mechanism described above does not prevent the possibility of inductor current ‘stair-casing’, an SOA mode is also featured. Rapid buildup of the device current can occur in the event of inductor saturation or when the input and output voltages are equal (no or very short inductor reset time).

The SOA mode is triggered whenever the device reaches current limit (I_{OCP}) and the on-time is less than t_{SOA}.

The SOA mode forces an off-time equal to t_{OCP} and pulls the internal error-voltage (V_E) down to approximately 1/2 of its set value.

Open FEEDBACK Pin Protection
The FEEDBACK pin also features a static current of I_{FB} that is continuously sourced out of the pin to protect against a fault related to an open FEEDBACK pin. The internal current source introduces a static offset to the output regulation which must be accounted for in selecting the output feedback regulation components.

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Hysteretic Thermal Shutdown

The thermal shutdown circuitry senses the controller die temperature. The threshold is set at 117 °C typical with a 49 °C hysteresis. When the die temperature rises above this threshold (OTP) (117 °C +8/-7 °C), the controller initiates a fast soft-shutdown and remains disabled until the die temperature falls by ~49°C, at which point the device will re-initiate the soft-start sequence.

In the event an OTP is detected when the VOLTAGE MONITOR pin current is below I_{UV+} threshold, the device will initiate a soft-shutdown and remain disabled until all the conditions for the start-up (soft-start sequence) are satisfied. In this mode of operation the OTP hysteresis is disabled.

When soft-shutdown is initiated by an over-temperature fault (OTP) the brown-out timer delay ($t_{BROWN-OUT}$) is disabled. The behavior of OTP depends on the input voltage peak detected following the thermal fault. If the input peak voltage detected after the thermal fault is below I_{UV+}, OTP hysteresis is disabled, however if the peak input voltage after the thermal fault is above I_{UV+} then the OTP hysteresis is enabled prior to re-initiating the soft-start sequence.

The maximum time delay for soft-shutdown to occur after an OTP event is detected is $t_{REFRESH}$.

In the event the input voltage is reduced below the brown-in threshold and an OTP event occurs (no OTP hysteresis) and the input voltage is raised immediately above brown-in before the controller junction temperature falls below the OTP threshold, the controller will initiate a soft-start once the controller junction is just below the OTP threshold. Depending on the system thermal conditions, the controller could initiate OTP shutdown again because of insufficient time to cool down the controller. The OTP shutdown that occurs when the input voltage is above brown-in will have hysteresis enabled.

Output Power Table

eSIP Package						
Product	**Efficiency Power Mode R = 49.9 kΩ**			**Full Power Mode R = 24.9 kΩ**		
	Maximum Continuous Output Power Rating at 90 VAC[2]		**Peak Output Power Rating at 90 VAC[4]**	**Maximum Continuous Output Power Rating at 90 VAC[2]**		**Peak Output Power Rating at 90 VAC[4]**
	Minimum[3]	Maximum		Minimum[3]	Maximum	
PFS7323L	60 W	80 W	90 W	85 W	110 W	120 W
PFS7324L	80 W	110 W	120 W	100 W	130 W	150 W
PFS7325L	110 W	150 W	165 W	140 W	185 W	205 W
PFS7326H	140 W	185 W	205 W	180 W	230 W	260 W
PFS7327H	175 W	230 W	255 W	220 W	290 W	320 W
PFS7328H	210 W	280 W	310 W	270 W	350 W	385 W
PFS7329H	235 W	320 W	345 W	293 W	380 W	425 W

Table 2. Output Power Table.

Notes:
1. See Key Application considerations.
2. Maximum practical continuous power at 90 VAC in an open-frame design with adequate heat sinking, measured at 50 °C ambient.
3. Recommended lower range of maximum continuous power for **best light load efficiency**; HiperPFS-2 will operate and perform below this level.
4. Internal output power limit.

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Application Example

A High Efficiency, 350 W, 385 VDC Universal Input PFC
The circuit shown in Figure 14 is designed using a PFS7328H device from the HiperPFS-2 family of integrated PFC controllers. This design is rated for a continuous output power of 350 W and provides a regulated output voltage of 385 VDC nominal maintaining a high input power factor and overall efficiency from light load to full load.

Fuse F1 provides protection to the circuit and isolates it from the AC supply in case of a fault. Diode bridge BR1 rectifies the AC input. Capacitors C1, C2, C3, and C4 together with inductors L1, L2, and L3 form the EMI filter reducing the common mode and differential mode noise. Resistors R1, R2 and CAPZero, IC U2 are required to discharge the EMI filter capacitors once the circuit is disconnected. CAPZero eliminates static losses in R1 and R2 by only connecting these components across the input when AC is removed.

The boost converter stage consists of inductor L5, and the HiperPFS-2 IC U1. This converter stage works as a boost converter and controls the input current of the power supply while simultaneously regulating the output DC voltage. Diode D3 prevents a resonant build up of output voltage at start-up by bypassing inductor L5 while simultaneously charging output capacitor C13. Thermistor RT1 limits the inrush input current of the circuit at start-up and prevents saturation of L5. In most high-performance designs, a relay will be used to bypass the thermistor after start-up to improve power supply efficiency. Capacitor C10 is used for reducing the loop length and area of the output circuit to reduce EMI and overshoot of voltage across the drain and source of the MOSFET inside U1 at each switching instant.

The PFS7328H IC requires a regulated supply of 12 V for operation and must not exceed 15 V. Resistors R10, R11, R12, Zener diode VR1, and transistor Q2 form a series pass regulator that prevents the supply voltage to IC U1 from exceeding 12 V. Capacitors C6, and C9 filter the supply voltage and provide decoupling to ensure reliable operation of IC U1. Diode D5 provides reverse polarity protection.

Resistor R15 programs the output voltage level [via the POWER GOOD THRESHOLD (PGT) pin] below which the POWER GOOD [PG] pin will go into a high-impedance state. IC U1 is configured in full power mode by resistor R14. Capacitor C8 decouples REFERENCE pin of IC U1.

The rectified AC input voltage of the power supply is sensed by IC U1 using resistors R7, R8 and R9. The capacitor C7 filters any noise on this signal.

Divider network comprising of resistors R18, R19, R20, and R21 are used to scale the output voltage and provide feedback to IC U1. Capacitor C14 enables rapid correction of output voltage overshoot or undershoot resulting from transient loading.

Resistor R17, R16, and capacitors C12 and C11 are required for shaping the loop response of the feedback network. The combination of resistor R16 and capacitor C12 provide a low frequency zero and the resistor R17, R16 and capacitor C12 form a low frequency pole. C15 and R22 attenuate high-frequency noise.

Diode D6 protects against an accidentally shorted capacitor C12 by safely shutting down the IC.

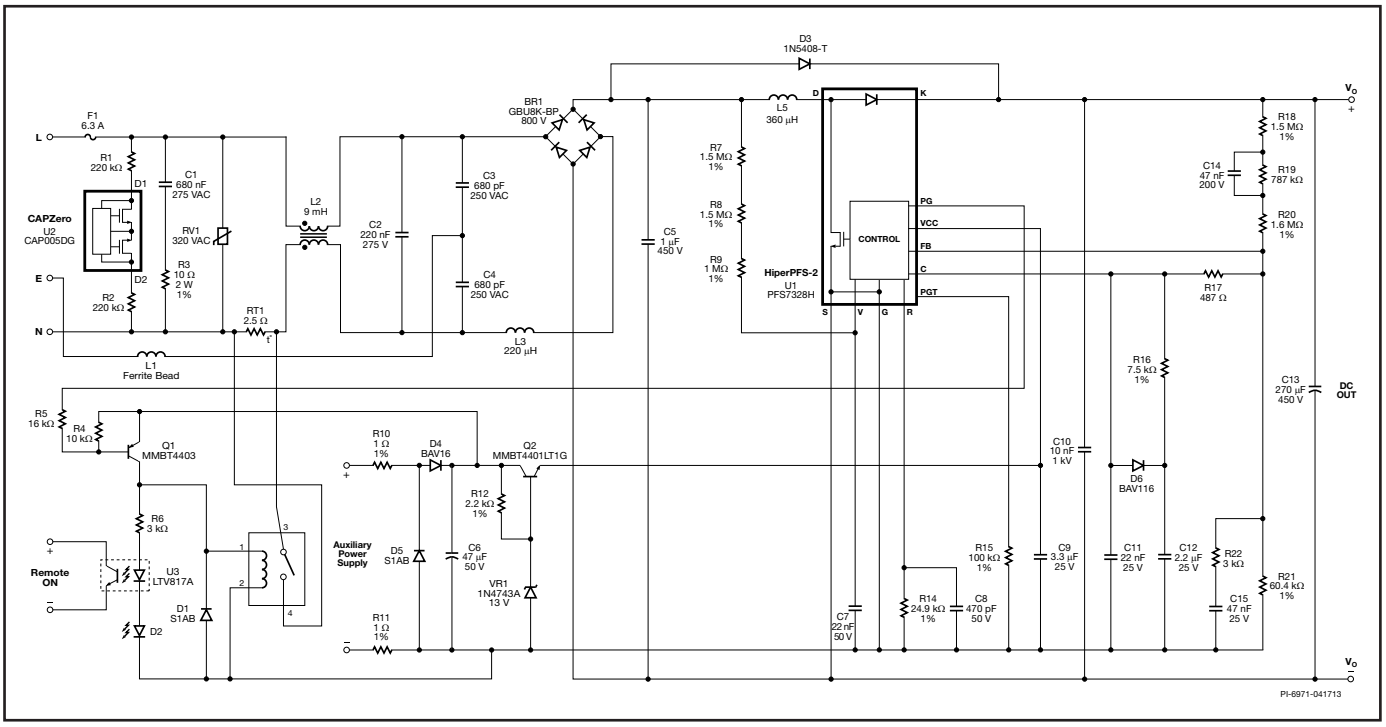

Figure 14. 350 W PFC using PFS7328H.

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Design, Assembly, and Layout Considerations

Power Table

The data sheet power table as shown in Table 2 represents the maximum practical continuous output power based on the following conditions:

For the universal input devices (PFS7323L-PFS7329H):

1. An input voltage range of 90 VAC to 264 VAC.
2. Overall efficiency of at least 93% at the lowest operating voltage.
3. 385 V nominal output.
4. Sufficient heat sinking to keep device temperature ≤100 ºC.

Operation beyond the limits stated above will require derating.

Use of a nominal output voltage higher than 390 V is not recommended for HiperPFS-2 based designs. Operation at voltages higher than 390 V can result in higher than expected drain-source voltage during line and load transients.

HiperPFS-2 Selection

Selection of the optimum HiperPFS-2 part depends on required maximum output power, PFC efficiency and overall system efficiency (when used with a second stage DC-DC converter), heat sinking constraints, system requirements and cost goals. The HiperPFS-2 part used in a design can be easily replaced with the next higher or lower part in the power table to optimize performance, improve efficiency or for applications where there are thermal design constraints. Minor adjustments to the inductance value and EMI filter components may be necessary in some designs when the next higher or the next lower HiperPFS-2 part is used in an existing design for performance optimization.

Every HiperPFS-2 family part has an optimal load level where it offers the most value. Operating frequency of a part will change depending on load level. Change of frequency will result in change in peak-to-peak current ripple in the inductance used. Change in current ripple will affect input PF and total harmonic distortion of input current.

Input Fuse and Protection Circuit

The input fuse should be rated for a continuous current above the input current at which the PFC turns-off due to input under voltage. This voltage is referred to as the brown-out voltage.

The fuse should also have sufficient I^2t rating in order to avoid nuisance failures during start-up. At start a large current is drawn from the input as the output capacitor charges to the peak of the applied voltage. The charging current is only limited by any inrush limiting thermistors, impedance of the EMI filter inductors, ESR of output capacitor and the forward resistance of the input rectifier diodes.

A MOV will typically be required to protect the PFC from line surges. Selection of the MOV rating will depend on the energy level (EN1000-4-5 Class level) to which the PFC is required to withstand.

A suitable NTC thermistor should be used on the input side to provide inrush current limiting. Choice of this thermistor should be made depending on the inrush current specification for the power supply. NTC thermistors may not be placed in any other location in the circuit as they fail to limit the stress on the part in the event of line transients and also fail to limit the inrush current in a predictable manner. Example shown in Figure 14 shows the circuit configuration that has the inrush limiting NTC thermistor on the input side which is bypassed with a relay after PFC start-up. This arrangement ensures that a consistent inrush limiting performance is achieved by the circuit.

Input EMI Filter

The variable switching frequency of the HiperPFS-2 effectively modulates the switching frequency and reduces conducted EMI peaks associated with the harmonics of the fundamental switching frequency. This is particularly beneficial for the average detection mode used in EMI measurements.

The PFC is a switching converter and will need an EMI filter at the input in order to meet the requirements of most safety agency standards for conducted and radiated EMI. Typically a common mode filter with X capacitors connected across the line will provide the required attenuation of high frequency components of input current to an acceptable level. The leakage reactance of the common mode filter inductor and the X capacitors form a low pass filter. In some designs, additional differential filter inductors may have to be used to supplement the differential inductance of the common mode choke.

A filter capacitor with low ESR and high ripple current capability should be connected at the output of the input bridge rectifier. This capacitor reduces the generation of the switching frequency components of the input current ripple and simplifies EMI filter design. Typically, 0.33 μF per 100 W should be used for universal input designs and 0.15 μF per 100 W of output power should be used for 230 VAC only designs.

It is often possible to use a higher value of capacitance after the bridge rectifier and reduce the X capacitance in the EMI filter.

Regulatory requirements require use of a discharge resistor to be connected across the input (X) capacitance on the AC side of the bridge rectifier. This is to ensure that residual charge is dissipated after the input voltage is removed when the capacitance is higher than 0.1 μF. Use of CAPZero integrated circuits from Power Integrations, helps eliminate the steady-state losses associated with the use of discharge resistors connected permanently across the X capacitors.

Inductor Design

It is recommended that the inductor be designed with the maximum operating flux density less than 0.3 T and a peak flux density less than 0.39 T at maximum current limit when a ferrite core is used. If a core made from Sendust or MPP is used, the flux density should not exceed 1 T. A powder core inductor will have a significant drop in inductance when the flux density approaches 1 T.

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For high performance designs, use of Litz wire is recommended to reduce copper loss due to skin effect and proximity effect. For toroidal inductors the numbers of layers should be less than 3 and for bobbin wound inductors, inter layer insulation should be used to minimize inter layer capacitance. For ferrite core inductor, a nominal K_P value of 0.35 is recommended for an optimal design. For Sendust core inductor, a nominal K_P value of 0.6 is recommended for an optimal design.

Output Capacitor

For a 385 V nominal PFC, use of a electrolytic capacitor with 450 V or higher continuous rating is recommended. The capacitance required is dependent on the acceptable level of output ripple and any hold-up time requirements. The equations below provide an easy way to determine the required capacitance in order to meet the hold-up time requirement and also to meet the output ripple requirements. The higher of the two values would be required to be used.

Capacitance required for meeting the hold-up requirement is calculated using the equation:

$$C_O = \frac{2 \times P_{OUT} \times t_{HOLD_UP}}{V_{OUT}^2 - V_{OUT(MIN)}^2}$$

C_O PFC output capacitance in F.
P_O PFC output power in watts.
$t_{HOLD-UP}$ Hold-up time specification for the power supply in seconds.
V_{OUT} Lowest nominal output voltage of the PFC in volts.
$V_{OUT(MIN)}$ Lowest permissible output voltage of the PFC at the end of hold-up time in volts.

Capacitance required for meeting the low frequency ripple specification is calculated using the equation:

$$C_O = \frac{I_{O(MAX)}}{2 \times \pi \times f_L \times \Delta V_L \times \eta_{PFC}}$$

f_L Input frequency in Hz.
ΔV_O Peak-peak output voltage ripple in volts.
η_{PFC} PFC operating efficiency.
$I_{O(MAX)}$ Maximum output current in amps.

Capacitance calculated using the above method should be appropriately increased to account for ageing and tolerances.

Power Supply for the IC

A 12 V regulated supply should be used for the HiperPFS-2. If the VCC exceeds 15 V, the HiperPFS-2 may be damaged. In most applications a simple series pass linear regulator made using an NPN transistor and Zener diode is adequate since the HiperPFS-2 only requires approximately 3.4 mA maximum for its operation.

It is recommended that a 3.3 µF or higher, low ESR ceramic capacitor be used to decouple the VCC supply. This capacitor should be placed directly at the IC on the circuit board.

Line-Sense Network

The line-sense network connected to the VOLTAGE MONITOR pin provides input voltage information to the HiperPFS-2. The value of this resistance sets the brown-in and brown-out threshold for the part. A value of 4 MΩ is recommended for use with the universal input parts. Only 1% tolerance resistors are recommended. This resistance value may be modified to adjust the brown-in threshold if required however change of this value will affect the maximum power delivered by the part.

A decoupling capacitor of 22 nF is required to be connected from the VOLTAGE MONITOR pin to the GROUND pin of the HiperPFS-2 for the universal input parts. This capacitor should be placed directly at the IC on the circuit board.

Feedback Network

A resistor divider network that provides 6 V at the FEEDBACK pin at the rated output voltage should be used. The compensation elements are included with the feedback divider network since the HiperPFS-2 does not have a separate pin for compensation. The HiperPFS-2 based PFC has two loops in its feedback. It has an inner current loop and a low bandwidth outer voltage loop which ensures high input power factor. The compensation RC circuit included with the feedback network reduces the response time of the HiperPFS-2 to fast changes in output voltage resulting from transient loads.

The recommended circuit and the associated component values are shown in Figure 15.

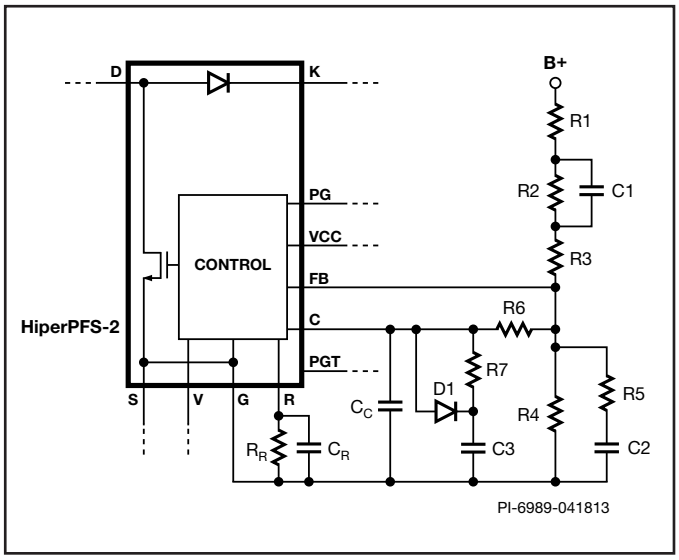

Figure 15. Recommended Feedback Circuit.

Resistors R1 to R4 comprise of the main output voltage divider network. The sum of resistors R1, R2 and R3 is the upper divider resistor and the lower feedback resistor is R4. Capacitor C1 is a soft-finish capacitor that reduces output voltage overshoot at start-up. Capacitor C_C is to filter any switching noise from coupling into the COMPENSATION pin. Resistor R7 and capacitor C3 is the loop compensation network which

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introduces a low frequency zero required to tailor the loop response to ensure low cross-over frequency and sufficient phase margin. Resistor R6 isolates the fast portion (resistor voltage divider network comprising of resistors R1 to R4) and the slow feedback loop compensator circuit (resistor R7 and capacitor C3). Diode D1 is included to cover a single point fault condition wherein capacitor C3 is shorted. In the event C3 is short-circuited, the FEEDBACK pin is forced below the FB_{OFF} threshold through diode D1 and subsequently turns the HiperPFS-2 off. Only a standard recovery diode should be used for D1. Use of ultrafast or fast recovery diode is not recommended including small signal diodes (e.g. 1N4148), which are typically also fast recovery.

The recommended values for the components used are as follows:

R4 = 60.4 kΩ
R3 = 1.6 MΩ
R2 = 787 kΩ
C1 = 47nF, 200 V X7R/NPO
R6 = 487 kΩ
R7 = 7.5 kΩ
C3 = 2.2 µF
Cc = 22 nF
D1 = BAV116 W or 1N4007 (A general purpose standard recovery diode should only be used).

When the above component values are used, the value of resistor R1 can be calculated using the following equation:

$$R_1 = \frac{V_O - 75}{100 \times 10^{-6}} - R_3$$

The value of resistor R7 will have to be adjusted in some designs and as a guideline the value from the following calculation can be used:

$$R_7 = R_Z = \frac{P_O}{1.2 \times V_O^2 \times C_O}(k\Omega)$$

P_O Maximum continuous output power in watts
V_O Nominal PFC output voltage in volts
C_O PFC output capacitance in farads

Improvement in low frequency phase margin can be achieved by increasing the value of the capacitor C3 however increase in value of capacitor C3 will result in some increase in overshoot at the output of the PFC during transient loading and should be verified.

Heat Sinking and Thermal Design
Figure 16, 17, 18 shows examples of the recommended assembly for the HiperPFS-2. In these assemblies as shown, no insulation pad is required and HiperPFS-2 can be directly connected to heat sink by clip or adhesive thermal material.

The HiperPFS-2 back metal is electrically connected to the heat sink and the heat sink is required to be connected to the HiperPFS-2 source terminal in order to reduce EMI.

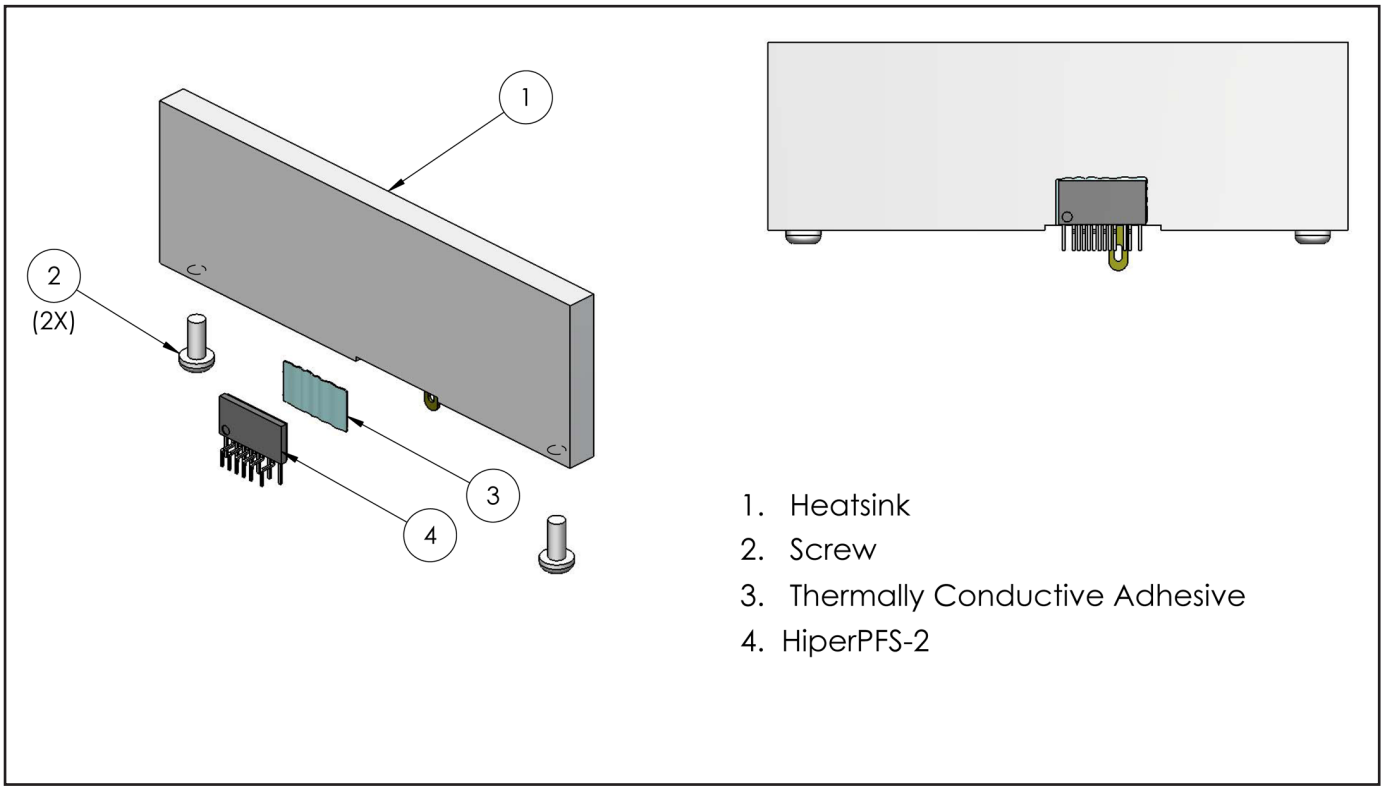

Figure 16. Heat Sink Assembly – Using Thermally Conductive Adhesive.

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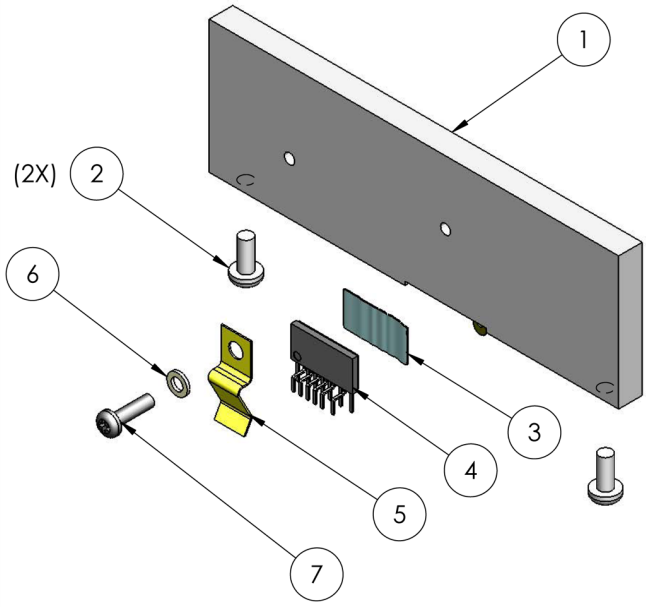
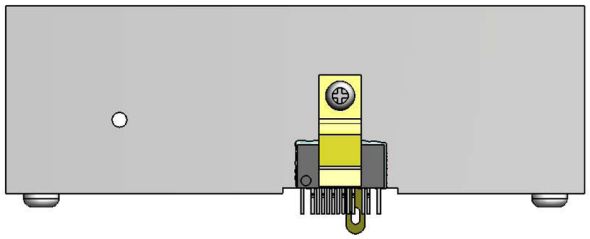
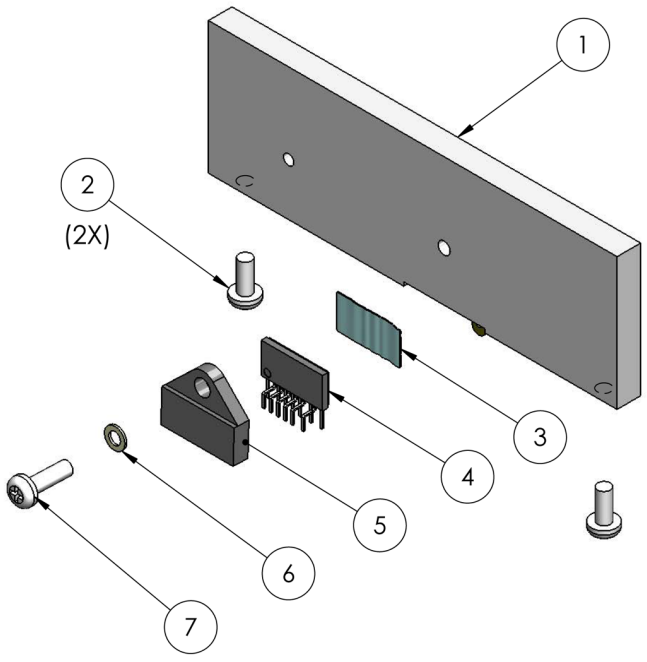
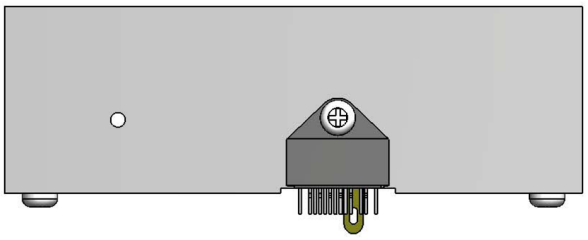




1. Heatsink
2. Screw
3. Thermally Conductive Silicone Grease
4. HiperPFS-2
5. Metal Clip
6. Lock Washer
7. Screw

Figure 17. Heat Sink Assembly – With Metal Clip.





1. Heatsink
2. Screw
3. Thermally Conductive Silicone Grease.
4. HiperPFS-2
5. Plastic Clip
6. Lock Washer
7. Screw

Figure 18. Heat Sink Assembly – With Plastic Clip.

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PCB Design Guidelines and Design Example

The line-sense network and the feedback circuit use large resistance values in order to minimize power dissipation in the feedback network and the line-sense network. Care should be taken to place the feedback circuit and the line-sense network components away from the high-voltage and high current nodes to minimize any interference. Any noise injected in the feedback network or the line-sense network will typically manifest as degradation of power factor. Excessive noise injection can lead to waveform instability or dissymmetry.

The EMI filter components should be clustered together to improve filter effectiveness. The placement of the EMI filter components on the circuit board should be such that the input circuit is located away from the drain node of the, or the PFC inductor.

A filter or decoupling capacitor should be placed at the output of the bridge rectifier. This capacitor together with the X capacitance in the EMI filter and the differential inductance of the EMI filter section and the source impedance, works as a filter to reduce the switching frequency current ripple in the input current. This capacitor also helps to minimize the loop area of the switching frequency current loop thereby reducing EMI.

The connection between the HiperPFS-2 drain node, output diode drain terminal and the PFC inductor should be kept as small as possible.

A low-loss ceramic dielectric capacitor should be connected between the cathode of the PFC output diode and the source terminal of the HiperPFS-2. This ensures that the loop area of the loop carrying high frequency currents at the transition of switch-off of the MOSFET is small and helps to reduce radiated EMI due to high frequency pulsating nature of the diode current traversing through the loop.

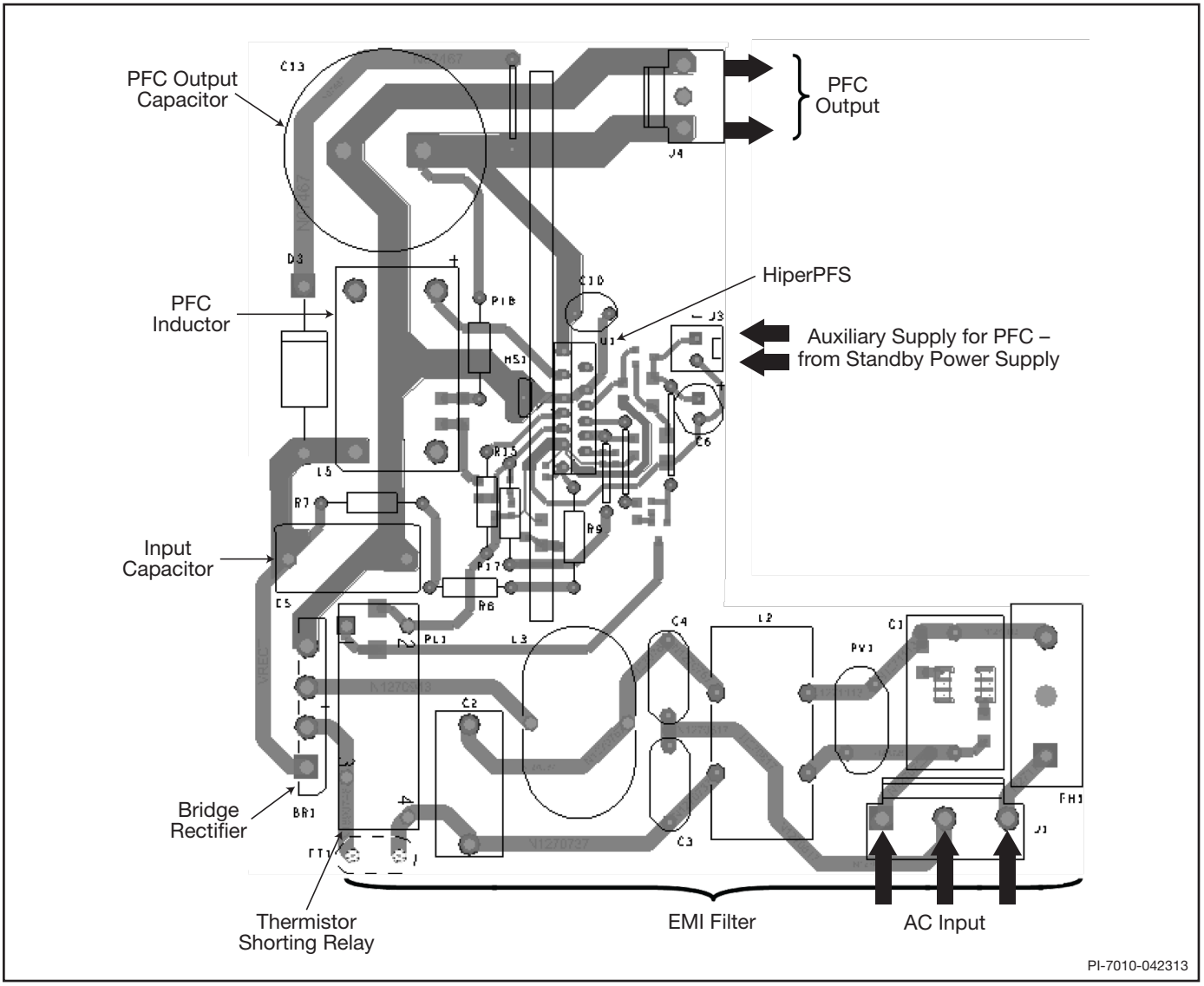

Figure 19. PCB Layout Example for System Power Supply Consisting of a PFC and a Second Stage Converter.

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During placement of components on the board, it is best to place the VOLTAGE MONITOR pin, FEEDBACK pin and VCC pin decoupling capacitors close to the HiperPFS-2 before the other components are placed and routed. Power supply return trace from the GROUND pin should be separate from the trace connecting the feedback circuit components to the GROUND pin. To minimize effect of trace impedance affecting regulation, output feedback should be taken directly from the output capacitor positive terminal. The upper end of the line-sense resistors should be connected to the high frequency filter capacitor connected at the output of the bridge rectifier.

Quick Design Checklist

As with any power supply design, all HiperPFS-2 designs should be verified on the bench to make sure that component specifications are not exceeded under worst-case conditions. The following minimum set of tests is strongly recommended:

1. Maximum drain voltage – verify that peak VDS does not exceed 530 V at lowest input voltage and maximum overload output power. Maximum overload output power occurs when the output is overloaded to a level just above the highest rated load or before the power supply output voltage starts falling out of regulation. Additional external snubbers should be used if this voltage is exceeded. In most designs, addition of a ceramic capacitor in the range of 33 pF and 100 pF connected across the PFC output diode will reduce the maximum drain-source voltage to a level below the BVDSS rating. When measuring drain-source voltage of the MOSFET, a high voltage probe should be used. When the probe tip is removed, a silver ring in the vicinity of the probe tip can be seen. This ring is at ground potential and the best ground connection point for making noise free measurements. Wrapping stiff wire around the ground ring and then connecting that ground wire into the circuit with the shortest possible wire length, and connecting the probe tip to the point being measured, ensures error-free measurement. Probe should be compensated according to probe manufacturers guidelines to ensure error-free measurement.
2. Maximum drain current – Drain current can be measured indirectly by monitoring inductor current. A current probe should be inserted between the bridge rectifier and inductor connection. At maximum ambient temperature, minimum input voltage and maximum output load, verify inductor current waveforms at start-up for any signs of inductor saturation. When performing this measurement with Sendust inductor, it is typical to see inductor waveforms that show exponential increase in current due to permeability drop. This should not be confused with hard saturation.
3. Thermal check – at maximum output power, minimum input voltage and maximum ambient temperature; verify that temperature specifications are not exceeded for the HiperPFS-2, PFC inductor, output diodes and output capacitors. Enough thermal margin should be allowed for the part-to-part variation of the RDS(ON) of HiperPFS-2, as specified in the data sheet. A maximum package temperature of 100 °C under worst-case operating conditions is recommended to allow for these variations.
4. Input PF should improve with load, if performance is found to progressively deteriorate with loading then that is a sign of possible noise pickup by the VOLTAGE MONITOR pin circuit or the feedback divider network and the compensation circuit.

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Absolute Maximum Ratings[2]

DRAIN Pin Peak Current: PFS7323 ..... 7.5 A
PFS7324 ..... 9.0 A
PFS7325 ..... 11.3 A
PFS7326 ..... 13.5 A
PFS7327 ..... 15.8 A
PFS7328 ..... 18.0 A
PFS7329 ..... 21.0 A
DRAIN Pin Voltage ..... -0.3 V to 530 V / 540 V[5]
VCC, PG, PGT Pin Voltage ..... -0.3 V to 15 V
VCC Pin Current ..... 25 mA
VOLTAGE MONITOR Pin Voltage ..... -0.3 V to 9 V
FEEDBACK Pin Voltage ..... -0.3 V to 9 V
COMPENSATION Pin Voltage ..... -0.3 V to 9 V
REFERENCE Pin Voltage ..... -0.3 V to 9 V
Storage Temperature ..... -65 °C to 150 °C
Junction Temperature[3] ..... -40 °C to 150 °C
Lead Temperature[4] ..... 260 °C

Notes:
1. All voltages referenced to SOURCE, T_A = 25 °C.
2. Maximum ratings specified may be applied one at a time without causing permanent damage to the product. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect product reliability.
3. Normally limited by internal circuitry.
4. 1/16 in. from case for 5 seconds.
5. Limited to a duration ≤ 15 ns and at a drain current ≤ $I_{LIM(TYP)}$.

Qspeed Diode

Peak Repetitive Reverse Voltage (V_{RRM})		530 V
Average Forward Current ($I_{F(AVG)}$)	$T_{J(D)}$ = 150 °C	3 A
Non-Repetitive Peak Surge Current (I_{FSM})	60 Hz, ½ cycle, $T_{C(D)}$ = 25 °C	50 A
Non-Repetitive Peak Surge Current (I_{FSM})	500 µs, $T_{C(D)}$ = 25 °C	130 A

Thermal Resistance

Thermal Resistance: H/L Package:
(θ_{JA})[1] ..... 103 °C/W
(θ_{JC}) ..... (see Figure 20)

Notes:
1. Controller junction temperature (T_{JI}) may be less than the Internal Power MOSFET Junction Temperature ($T_{J(M)}$) and Diode Junction Temperature ($T_{J(D)}$).

Parameter	Symbol	Conditions SOURCE = 0 V; V_{CC} = 12 V, T_{JI} = -40 °C to 125 °C (Note C) (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions							
Maximum Operating ON-time	$t_{ON(MAX)}$	0 °C < T_{JI} < 100 °C		30	40	50	µs
Minimum Operating ON-time	$t_{ON(MIN)}$	0 °C < T_{JI} < 100 °C See Note A		0.5		1	
Maximum Operating OFF-time	$t_{OFF(MAX)}$	0 °C < T_{JI} < 100 °C		30	40	50	
Minimum Operating OFF-time	$t_{OFF(MIN)}$	0 °C < T_{JI} < 100 °C		1		3.5	
Internal Feedback Voltage Reference	V_{REF}	T_{JI} = 25 °C See Note A		5.955	6.00	6.045	V
COMPENSATION Pin Voltage	V_C	0 °C < T_{JI} < 100 °C (In Regulation)		5.88	6.00	6.12	V
FEEDBACK Pin Current	I_{FB}	T_{JI} = 25 °C	Normal Operation	340	500	640	nA
Soft-Start Time	t_{SOFT}	T_{JI} = 25 °		12			ms
Internal Compensation Frequency	f_{COMP}	See Note A Pole (fp)			1		kHz
Error-Amplifier Gain	A_v	See Note A			100		V/V

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Parameter	Symbol	Conditions SOURCE = 0 V; V_{CC} = 12 V, T_{JI} = -40 °C to 125 °C (Note C) (Unless Otherwise Specified)	Min	Typ	Max	Units
Line-Sense/Peak Detector						
Brown-In Threshold Current	I_{UV+}	0 °C < T_{JI} < 100 °C		27.50	28.88	µA
Brown-Out Threshold Current	I_{UV-}	0 °C < T_{JI} < 100 °C	22.52	24.50		µA
Brown-In/Out Hysteresis	$I_{UV(HYST)}$	0 °C < T_{JI} < 100 °C	2.5		5.5	µA
Soft-Start Brown-Out Threshold Current	$I_{UV(SS)}$	T_{JI} = 25 °C		20.62		µA
Soft-Start Brown-Out Time-Out	$t_{UV(SS)}$	T_{JI} = 25 °C	1000			ms
VOLTAGE MONITOR Pin Voltage Threshold	$V_{V(THR)}$	0 °C < T_{JI} < 100 °C I_V = I_{UV+}	1.6	2.3	3.1	V
VOLTAGE MONITOR Pin Short-Circuit Current	$I_{V(SC)}$	0 °C < T_{JI} < 100 °C V_V = 6 V		280		µA
VOLTAGE MONITOR Pin Pre-Soft-Start Current	$I_{V(SS)}$	0 °C < T_{JI} < 100 °C V_V = 3 V		5		mA
Line Sample Refresh Period	$t_{REFRESH}$	T_{JI} = 25 °C	16		60	ms
Brown-Out Timer	$t_{BROWN-OUT}$	T_{JI} = 25 °C	32		60	ms
VOLTAGE MONITOR Pin Shutdown Current Threshold	$I_{V(OFF)}$	0 °C < T_{JI} < 100 °C		200		µA
VOLTAGE MONITOR Pin Shutdown Delay	$t_{V(OFF)}$	T_{JI} = 25 °C	65	110	135	µs

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Parameter	Symbol	Conditions SOURCE = 0 V; V_{CC} = 12 V, T_{JI} = -40 °C to 125 °C (Note C) (Unless Otherwise Specified)		Min	Typ	Max	Units
Current Limit/Circuit Protection							
Over-Current Protection	I_{OCP}	PFS7323L di/dt = 250 mA/µs T_{JI} = 25 °C	I_V < 48 µA	3.8	4.1	4.3	
			I_V > 59 µA	2.5	2.9	3.2	
		PFS7324L di/dt = 300 mA/µs T_{JI} = 25 °C	I_V < 48 µA	4.5	4.8	5.1	
			I_V > 59 µA	3.0	3.5	3.8	
		PFS7325L di/dt = 400 mA/µs T_{JI} = 25 °C	I_V < 48 µA	5.5	5.9	6.2	
			I_V > 59 µA	3.7	4.2	4.7	
		PFS7326H di/dt = 500 mA/µs T_{JI} = 25 °C	I_V < 48 µA	6.8	7.2	7.5	
			I_V > 59 µA	4.6	5.2	5.7	
		PFS7327H di/dt = 650 mA/µs T_{JI} = 25 °C	I_V < 48 µA	8.0	8.4	8.8	
			I_V > 59 µA	5.4	6.0	6.6	
		PFS7328H di/dt = 800 mA/µs T_{JI} = 25 °C	I_V < 48 µA	9.0	9.5	9.9	
			I_V > 59 µA	6.0	6.6	7.3	
		PFS7329H di/dt = 920 mA/µs T_{JI} = 25 °C	I_V < 48 µA	10.0	10.5	11.0	
			I_V > 59 µA	6.6	7.4	7.9	
SOA Protection Time-Out	t_{OCP}	T_{JI} = 25 °C		265	315	365	µs
SOA On-time	t_{SOA}	T_{JI} = 25 °C See Note A				1	µs
Leading Edge Blanking (LEB) Time	t_{LEB}	See Note A			220		ns
Current Limit Delay (ILD)	$t_{IL(D)}$	See Note A			100		ns
LEB + ILD + Driver Delay	$t_{LEB} + t_{IL(D)} + t_{DRIVER}$	T_{JI} = 25 °C		370	470	570	ns
Thermal Shutdown Temperature	T_{SHUT}	See Note A		110	117	125	°C
Thermal Shutdown Hysteresis	T_{HYST}	See Note A			49		°C
COMPENSATION Pin Undervoltage Threshold	C_{UV}	T_{JI} = 25 °C		3	3.5	4	V
COMPENSATION Pin Undervoltage Delay	$t_{C(UV)}$	T_{JI} = 25 °C		65	100	135	µs
Feedback Start-Up Threshold	FB_{OFF}	0 °C < T_{JI} < 100 °C		1.15	1.25	1.45	V
FEEDBACK Pin Off Delay	$t_{FB(OFF)}$	0 °C < T_{JI} < 100 °C			5		µs

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Parameter	Symbol	Conditions SOURCE = 0 V; V_{CC} = 12 V, T_{JI} = -40 °C to 125 °C (Note C) (Unless Otherwise Specified)		Min	Typ	Max	Units
Current Limit/Circuit Protection (cont.)							
COMPENSATION Pin Start-Up Threshold	C_{OFF}	0 °C < T_{JI} < 100 °C		0.5	1.2	1.65	V
COMPENSATION Pin Off Delay	$t_{C(OFF)}$	0 °C < T_{JI} < 100 °C			5		µs
FEEDBACK Pin Overvoltage Threshold	FB_{OV}	0 °C < T_{JI} < 100 °C Referenced to V_{REF}		V_{REF} +600 mV	V_{REF} +700 mV	V_{REF} +850 mV	V
COMPENSATION Pin Overvoltage Threshold	C_{OV}	0 °C < T_{JI} < 100 °C Referenced to V_{REF}		V_{REF} +25 mV	V_{REF} +90 mV	V_{REF} +160 mV	V
		0 °C < T_{JI} < 100 °C Hysterisis			50		mV
FEEDBACK Pin/ COMPENSATION Pin Overvoltage Delay	$t_{FB(OV)}$ $t_{C(OV)}$	0 °C < T_{JI} < 100 °C		1	2	3	µs
FEEDBACK Pin Overvoltage Hysteresis	$FB_{OV(HYST)}$	0 °C < T_{JI} < 100 °C			+300 mV		V
FEEDBACK Pin Overvoltage Offset Threshold	FBC_{OV}	0 °C < T_{JI} < 100 °C Referenced to V_C (COMPENSATION Pin)		V_C +225 mV	V_C +250 mV	V_C +275 mV	V
FEEDBACK Pin Undervoltage Offset Threshold	FBC_{UV}	0 °C < T_{JI} < 100 °C Referenced to V_C (COMPENSATION Pin)		V_C -275 mV	V_C -250 mV	V_C -215 mV	V
FEEDBACK Pin Charge Current	I_{FBC}	0 °C < T_{JI} < 100 °C $\lvert V_{FB}-V_C \rvert$ > 215 mV		2			mA
Start-Up V_{CC} (Rising Edge)	V_{CC+}	T_{JI} = 25 °C		9.5		10.2	V
VCC Operating Range	V_{CC}	T_{JI} = 25 °C, See Note A		10.2	12	13.2	V
Shutdown V_{cc} (Falling Edge)	V_{CC-}	T_{JI} = 25 °C		9.0		9.5	V
VCC Hysteresis	$VCC_{(HYST)}$	0 °C < T_{JI} < 100 °C		0.2	0.5	0.8	V
Supply Current Characteristics	I_{CD1}	0 °C < T_{JI} < 100 °C Switching				3.5	mA
	I_{CD2}	0 °C < T_{JI} < 100 °C Not Switching				2.5	
VCC Power-Up Reset Threshold	$V_{CC(POR)}$	T_{JI} = 25 °C		2.85	3.6	4.25	V
VCC Power-Up Reset Current	$I_{VCC(POR)}$	T_{JI} = 25 °C				2.5	mA
REFERENCE Pin Voltage	V_R	0 °C < T_{JI} < 100 °C R_{REF} = 24.9 kΩ		1.240	1.265	1.300	V
REFERENCE Pin Threshold	I_R	0 °C < T_{JI} < 100 °C	Full Power Mode (24.9 kΩ)	48.50	51.00	53.50	µA
			Efficiency Power Mode (49.9 kΩ)	24.00	25.50	27.00	

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Parameter	Symbol	Conditions SOURCE = 0 V; V_{CC} = 12 V, T_{JI} = -40 °C to 125 °C (Note C) (Unless Otherwise Specified)			Min	Typ	Max	Units
Current Limit/Circuit Protection (cont.)								
REFERENCE Pin Off-State Current Threshold	$I_{R(OFF)}$	T_{JI} = 25 °C See Figure 12	Short REFERENCE Pin to G/S		60			µA
			Open REFERENCE Pin				20	
Power Good								
Power Good Threshold Set Reference Current	I_{PGT}	0 °C < T_{JI} < 100 °C			48.5	51.0	53.5	µA
Power Good Delay Time	t_{PG}	T_{JI} = 25 °C					100	µs
Power Good Internal Reference Threshold (Start-Up Threshold)	$V_{PG(H)}$	0 °C < T_{JI} < 100 °C Reference to V_{REF}			V_{REF} -600 mV	V_{REF} -300 mV	V_{REF} -0 mV	V
POWER GOOD Pin Leakage Current in Off-State	$I_{PG(OFF)}$	T_{JI} = 25 °C V_{PGT} < V_{REF} – 0.3 V					500	nA
Power Good On-State Voltage	$V_{PG(ON)}$	T_{JI} = 25 °C I_{PG} = 2 mA					2	V
Power Good Comparator Input Offset Voltage	$V_{PG(OS)}$	0 °C < T_{JI} < 100 °C			-50		+50	mV
Power Good Threshold Operating Voltage	V_{PGT}	0 °C < T_{JI} < 100 °C See Note A			0		13.2	V
Power Good Operating Voltage	V_{PG}	0 °C < T_{JI} < 100 °C See Note A			0		13.2	V
Power MOSFET								
ON-State Resistance	$R_{DS(ON)}$	I_D = I_{OCP} × 0.5 and I_V < 48 µA	PFS7323	$T_{J(M)}$ = 25 °C		0.58	0.69	Ω
				$T_{J(M)}$ = 100 °C			1.10	
			PFS7324	$T_{J(M)}$ = 25 °C		0.49	0.58	
				$T_{J(M)}$ = 100 °C			0.92	
			PFS7325	$T_{J(M)}$ = 25 °C		0.39	0.46	
				$T_{J(M)}$ = 100 °C			0.73	
			PFS7326	$T_{J(M)}$ = 25 °C		0.33	0.39	
				$T_{J(M)}$ = 100 °C			0.62	
			PFS7327	$T_{J(M)}$ = 25 °C		0.28	0.33	
				$T_{J(M)}$ = 100 °C			0.52	
			PFS7328	$T_{J(M)}$ = 25 °C		0.25	0.29	
				$T_{J(M)}$ = 100 °C			0.46	
			PFS7329	$T_{J(M)}$ = 25 °C		0.21	0.25	
				$T_{J(M)}$ = 100 °C			0.40	

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Parameter	Symbol	Conditions SOURCE = 0 V; V_{CC} = 12 V, T_{JI} = -40 °C to 125 °C (Note C) (Unless Otherwise Specified)			Min	Typ	Max	Units
Power MOSFET (cont.)								
Effective Output Capacitance	C_{OSS}	$T_{J(M)}$ = 25 °C V_{GS} = 0 V, V_{DS} = 0 to 80% V_{DSS} (See Note A)		PFS7323			176	pF
				PFS7324			210	
				PFS7325			265	
				PFS7326			312	
				PFS7327			320	
				PFS7328			420	
				PFS7329			487	
Breakdown Voltage	BV_{DSS}	$T_{J(M)}$ = 25 °C, VCC = 12 V I_D = 250 µA, V_{FB} = V_V = V_C = 0 V			530			V
Breakdown Voltage Temperature Coefficient	$BV_{DSS(TC)}$					0.048		%/°C
Off-State Drain Current Leakage	I_{DSS}	$T_{J(M)}$ = 100 °C V_{DS} = 80% BV_{DSS} VCC = 12 V V_{FB}=V_V=V_C=0	PFS7323	$T_{J(M)}$ = 100 °C			80	µA
			PFS7324	$T_{J(M)}$ = 100 °C			100	
			PFS7325	$T_{J(M)}$ = 100 °C			120	
			PFS7326	$T_{J(M)}$ = 100 °C			150	
			PFS7327	$T_{J(M)}$ = 100 °C			170	
			PFS7328	$T_{J(M)}$ = 100 °C			200	
			PFS7329	$T_{J(M)}$ = 100 °C			235	
Turn-Off Voltage Rise Time	t_R	See Notes A, B, C				50		ns
Turn-On Voltage Fall Time	t_F					100		
Start-Up Time Delay	$t_{START-DELAY}$	0 °C < T_{JI} < 100 °C See Note A, B			2	6	10	ms

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Parameter	Symbol	Conditions SOURCE = 0 V; V_{CC} = 12 V, T_{JI} = -40 °C to 125 °C (Note C) (Unless Otherwise Specified)		Min	Typ	Max	Units
Qspeed Diode							
DC Characteristics							
Reverse Current	$I_{R(D)}$	V_R = 530 V, $T_{J(D)}$ = 25 °C			0.4		µA
		V_R = 530 V, $T_{J(D)}$ = 100 °C			0.07		mA
Forward Voltage	V_F	I_F = 3 A, $T_{J(D)}$ = 25 °C			1.55		V
		I_F = 3 A, $T_{J(D)}$ = 100 °C			1.47		
Junction Capacitance	C_J	V_R = 10 V, 1 MHz			18		pF
Dynamic Characteristics							
Reverse Recovery Time	t_{RR}	di/dt = 200 A/µs, VR = 400 V IF = 3 A	$T_{J(D)}$ = 25 °C		25		ns
			$T_{J(D)}$ = 100 °C		31		
Reverse Recovery Charge	Q_{RR}	di/dt = 200 A/µs, VR = 400 V IF = 3 A	$T_{J(D)}$ = 25 °C		33.5		nC
			$T_{J(D)}$ = 100 °C		57		
Maximum Reverse Recovery Current	I_{RRM}	di/dt = 200 A/µs, VR = 400 V IF = 3 A	$T_{J(D)}$ = 25 °C		1.9		A
			$T_{J(D)}$ = 100 °C		2.5		
Softness Factor = t_B/t_A	S	di/dt = 200 A/µs, VR = 400 V IF = 3 A	$T_{J(D)}$ = 25 °C		1		-
			$T_{J(D)}$ = 100 °C		0.45		

NOTES:

A. Not tested parameter. Guaranteed by design.

B. Tested in typical Boost PFC application circuit with 22 nF capacitor between VOLTAGE MONITOR and SIGNAL GROUND pins, and 4 MΩ resistor from rectified line to the VOLTAGE MONITOR pin.

C. Normally limited by internal circuitry.

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Typical Performance Characteristics

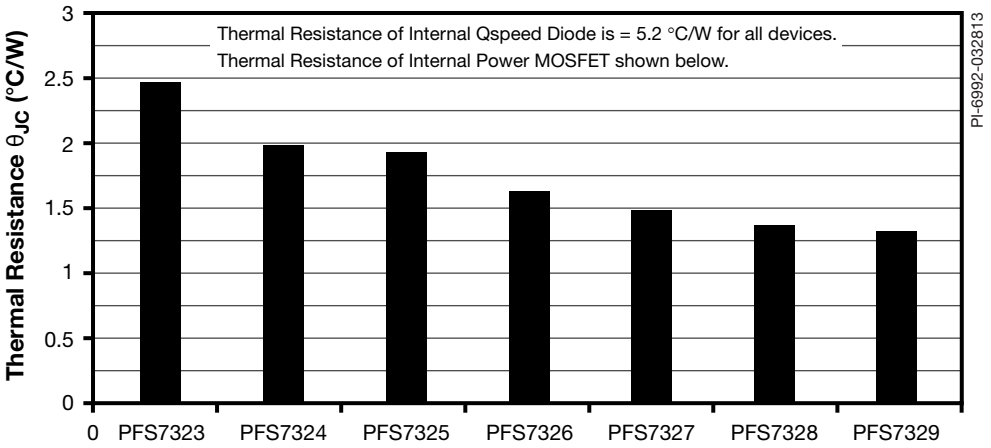

Figure 20. Thermal Resistance (θ_{JC}).

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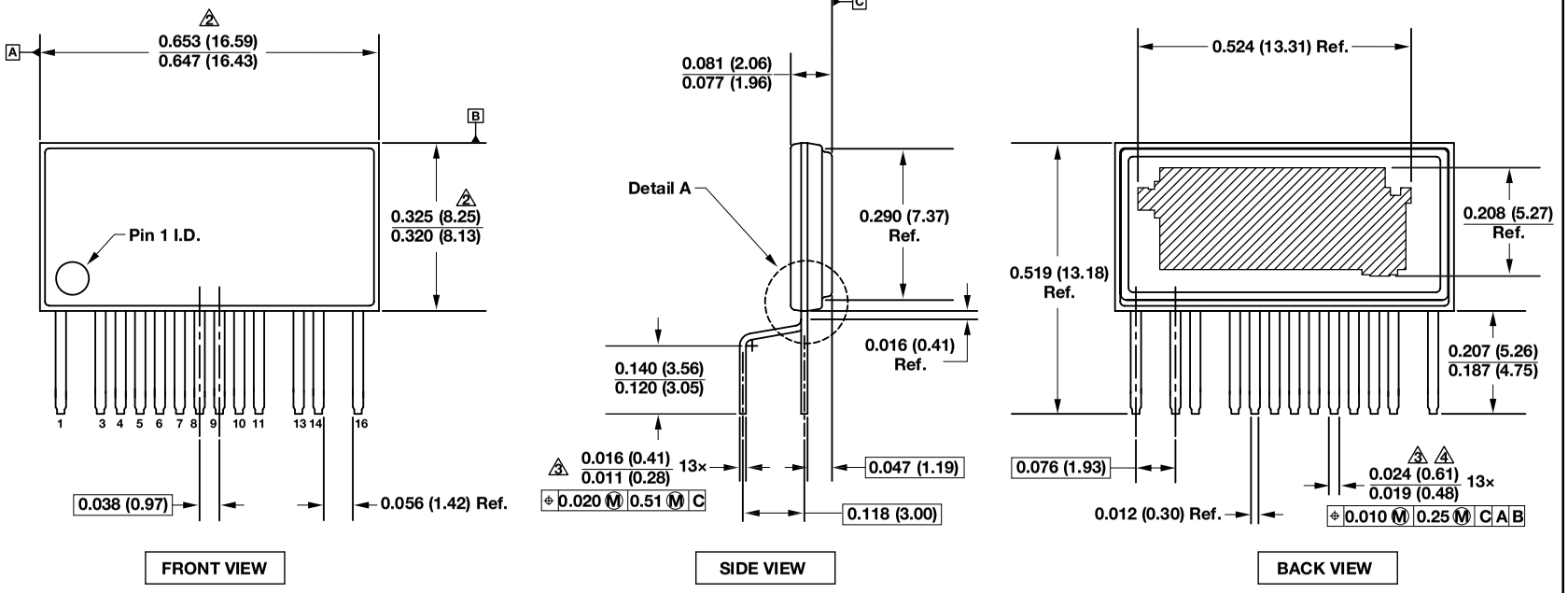
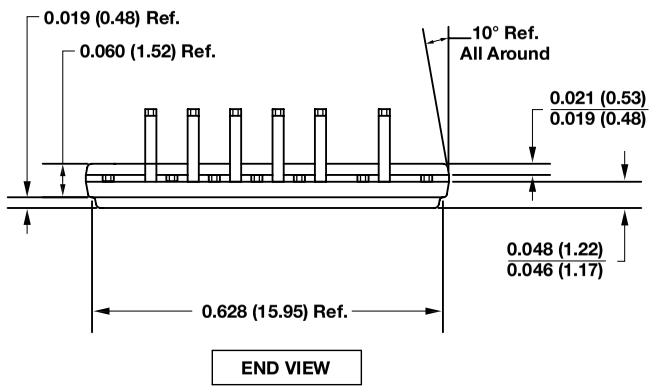
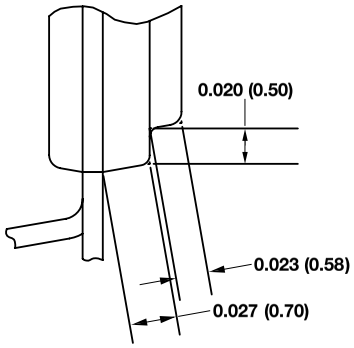
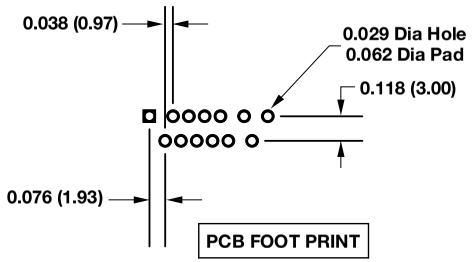
eSIP-16D (H Package)









Dimensions in inches, (mm).
All dimensions are for reference.

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.007 [0.18] per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include interlead flash or protrusions.
5. Controlling dimensions in inches (mm).

PI-6972-022713

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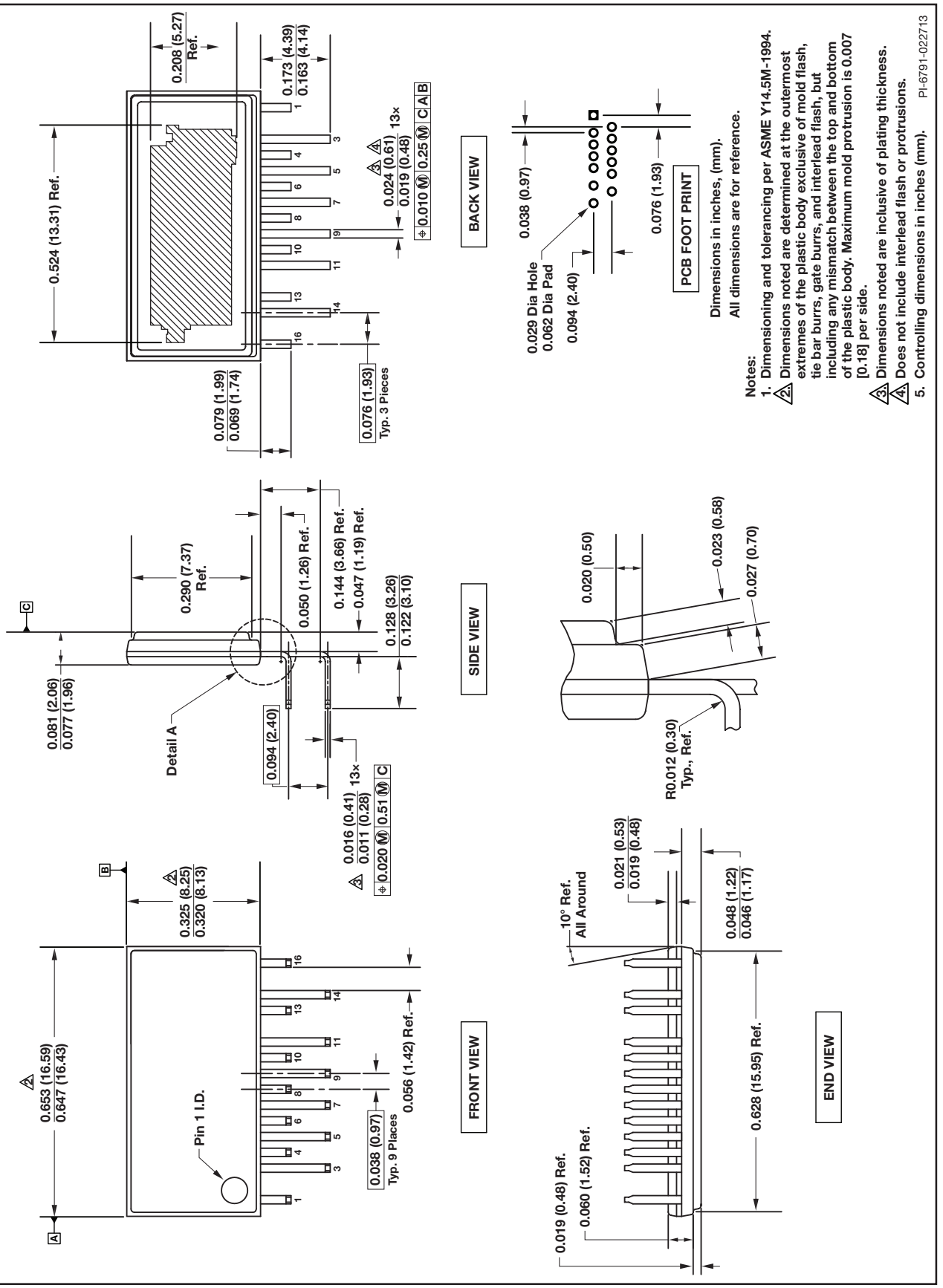
eSIP-16G (L Package)



Dimensions in inches, (mm).
All dimensions are for reference.

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.007 [0.18] per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include interlead flash or protrusions.
5. Controlling dimensions in inches (mm).

PI-6791-022713

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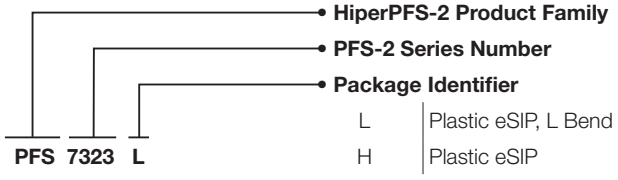
Part Ordering Information

Part Number	Option	Quantity
PFS7323L	Tube	30
PFS7324L	Tube	30
PFS7325L	Tube	30
PFS7326H	Tube	30
PFS7327H	Tube	30
PFS7328H	Tube	30
PFS7329H	Tube	30

Part Marking Information



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Revision	Notes	Date
A	Initial Release.	06/03/13
B	Updated $t_{BROWN-OUT}$. Updated Minimum I_{OCP} for PFS7329H.	06/10/13

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