PCK9456

2.5 V and 3.3 V LVCMOS clock fan-out buffer

Rev. 01 — 31 July 2006 Product data sheet

1. General description

The PCK9456 is a 2.5 V and 3.3 V compatible 1 : 10 clock distribution buffer designed for low voltage mid-range to high-performance telecommunications, networking and computing applications. Both 3.3 V, 2.5 V and dual supply voltages are supported for mixed voltage applications. The PCK9456 offers 10 low-skew outputs and a differential LVPECL clock input. The outputs are configurable and support 1 : 1 and 1 : 2 output to input frequency ratios. The PCK9456 is specified for the extended temperature range of –40 °C to +85 °C.

2. Features

- Configurable 10 outputs LVCMOS clock distribution buffer
- Compatible to single, dual and mixed 3.3 V/2.5 V voltage supply
- Wide range output clock frequency up to 250 MHz
- Designed for mid-range to high performance telecommunications, networking and computer applications
- Supports high performance differential clocking applications
- Maximum output skew of 200 ps (150 ps within one bank)
- Selectable output configurations per output bank
- 3-stateable outputs
- Available in LQFP32 package
- Ambient operating temperature of –40 °C to +85 °C

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCK9456BD	LQFP32	plastic low profile quad flat package; 32 leads; body 7 × 7 × 1.4 mm	SOT358-1

PHILIPS

4. Functional diagram

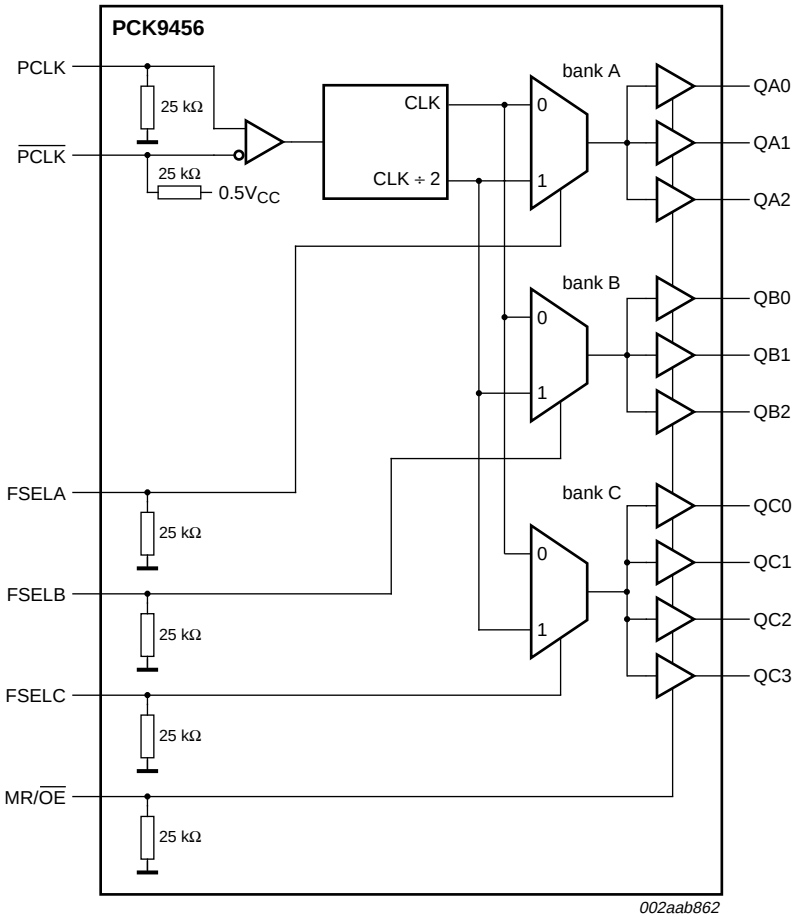


Fig 1. Functional diagram of PCK9456

5. Pinning information

5.1 Pinning

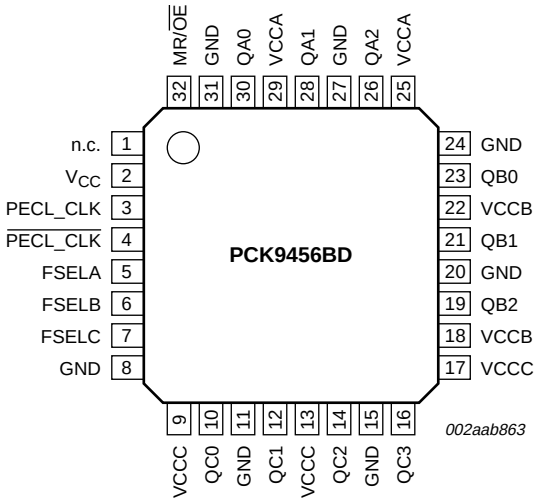


Fig 2. Pin configuration for LQFP32

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Type	Description
PECL_CLK	3	LVPECL	differential clock reference
$\overline{\text{PECL\_CLK}}$	4	LVPECL	low voltage positive ECL input
FSELA	5	LVCMOS	output bank divide select input
FSELB	6	LVCMOS	
FSELC	7	LVCMOS	
GND	8, 11, 15, 20, 24, 27, 31	supply	ground
VCCA	25, 29	supply	positive voltage supply for output bank A
VCCB	18, 22	supply	positive voltage supply for output bank B; internally connected to V_{CC}
VCCC	9, 13, 17	supply	positive voltage supply for output bank C
V_{CC}	2	supply	positive voltage supply core (V_{CC})
QA0, QA1, QA2	30, 28, 26	LVCMOS	bank A outputs
QB0, QB1, QB2	23, 21, 19	LVCMOS	bank B outputs
QC0, QC1, QC2, QC3	10, 12, 14, 16	LVCMOS	bank C outputs
MR/$\overline{\text{OE}}$	32	LVCMOS	internal reset and output 3-state control
n.c.	1	-	not connected

6. Functional description

The PCK9456 is a full static design supporting clock frequencies up to 250 MHz. The signals are generated and re-timed on-chip to ensure minimal skew between the three output banks (see Figure 1 “Functional diagram of PCK9456”).

Each of the three output banks can be individually supplied by 2.5 V or 3.3 V, supporting mixed voltage applications. The FSELx pins choose between division of the input reference frequency by one or two. The frequency divider can be set individually for each of the three output banks. The PCK9456 can be reset and the outputs are disabled by deasserting the MR/$\overline{OE}$ pin (logic HIGH state). Asserting MR/$\overline{OE}$ will enable the outputs.

All control inputs accept LVCMOS signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines. The clock input is low voltage PECL compatible for differential clock distribution support. Please consult the PCK9446 specification for a full CMOS compatible device. For series terminated transmission lines, each of the PCK9456 outputs can drive one or two traces, giving the devices an effective fan-out of 1 : 20. The device is packaged in a 7 mm × 7 mm LQFP32 package.

Table 3 details the supported single and dual supply configurations.

Table 3. Supported single and dual supply configurations

Supply voltage configuration	V_{CC}[1]	$V_{CC(bankA)}$[2]	$V_{CC(bankB)}$[3]	$V_{CC(bankC)}$[4]	GND
3.3 V	3.3 V	3.3 V	3.3 V	3.3 V	0 V
Mixed voltage supply	3.3 V	3.3 V or 2.5 V	3.3 V	3.3 V or 2.5 V	0 V
2.5 V	2.5 V	2.5 V	2.5 V	2.5 V	0 V

[1] V_{CC} is the positive power supply of the device core and input circuitry. V_{CC} voltage defines the input threshold and levels.

[2] $V_{CC(bankA)}$ is the positive power supply of the bank A outputs. $V_{CC(bankA)}$ voltage defines bank A output levels.

[3] $V_{CC(bankB)}$ is the positive power supply of the bank B outputs. $V_{CC(bankB)}$ voltage defines the bank B output levels. $V_{CC(bankB)}$ is internally connected to V_{CC}.

[4] $V_{CC(bankC)}$ is the positive power supply of the bank C outputs. $V_{CC(bankC)}$ voltage defines bank C output levels.

6.1 Function table

Table 4. Function table (controls)

Control	Default	0	1
FSELA	0	QA[0:2] frequency = f_{ref}	QA[0:2] frequency = $f_{ref} \div 2$
FSELB	0	QB[0:2] frequency = f_{ref}	QB[0:2] frequency = $f_{ref} \div 2$
FSELC	0	QC[0:3] frequency = f_{ref}	QC[0:3] frequency = $f_{ref} \div 2$
MR/$\overline{OE}$	0	outputs enabled	internal reset; outputs disabled (3-state)

7. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		–0.3	+4.6	V
V_I	input voltage		–0.3	V_{CC} + 0.3	V
V_O	output voltage		–0.3	V_{CC} + 0.3	V
I_I	input current		-	±20	mA
I_O	output current		-	±50	mA
T_{stg}	storage temperature		–40	+125	°C

8. Recommended operating conditions

Table 6. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.375	-	3.465	V
$V_{CC(bankA)}$	supply voltage (bank A)	VCCA pins	2.375	-	3.465	V
$V_{CC(bankB)}$	supply voltage (bank B)	VCCB pins	2.375	-	3.465	V
$V_{CC(bankC)}$	supply voltage (bank C)	VCCC pins	2.375	-	3.465	V
T_{amb}	ambient temperature		–40	-	+85	°C

9. Characteristics

Table 7. General characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_T	termination voltage	output	-	$0.5V_{CC}$	-	V
V_{esd}	electrostatic discharge voltage	MM	200	-	-	V
		HBM	2000	-	-	V
$I_{latch(prot)}$	latch-up protection current		200	-	-	mA
C_{PD}	power dissipation capacitance	per output	-	10	-	pF
C_i	input capacitance		-	4.0	-	pF

Table 8. Static characteristics (3.3 V)

T_{amb} = −40 °C to +85 °C; V_{CC} = $V_{CC(bankA)}$ = $V_{CC(bankB)}$ = $V_{CC(bankC)}$ = 3.3 V ± 5 %

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage	LVCMOS		2.0	-	V_{CC} + 0.3	V
V_{IL}	LOW-level input voltage	LVCMOS		−0.3	-	+0.8	V
$V_{i(p-p)}$	peak-to-peak input voltage	PCLK; LVPECL		250	-	-	V
V_{ICR}	common mode input voltage range	PCLK; LVPECL	[1]	1.1	-	V_{CC} − 0.6	V
I_I	input current	V_I = GND or V_I = V_{CC}	[2]	-	-	±200	µA
V_{OH}	HIGH-level output voltage	I_{OH} = −24 mA	[3]	2.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 24 mA	[2]	-	-	0.55	V
		I_{OL} = 12 mA		-	-	0.30	
Z_o	output impedance			-	14 to 17	-	Ω
$I_{CC(max)}$	maximum supply current	all V_{CC} pins	[4]	-	-	2.0	mA

[1] V_{ICR} (DC) is the crossing point of the differential input signal. Functional operation is obtained when the crossing point is within the V_{ICR} range and the input swing lies within the $V_{i(p-p)}$ (DC) specification.

[2] Input pull-up/pull-down resistors influence input current.

[3] The PCK9456 is capable of driving 50 Ω transmission lines on the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of V_T. Alternatively, the device drives up to two 50 Ω series terminated transmission lines.

[4] $I_{CC(max)}$ is the DC current consumption of the device with all outputs open and the input in its default state or open.

Table 9. Static characteristics (2.5 V)

T_{amb} = −40 °C to +85 °C; V_{CC} = $V_{CC(bankA)}$ = $V_{CC(bankB)}$ = $V_{CC(bankC)}$ = 2.5 V ± 5 %

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage	LVCMOS		1.7	-	V_{CC} + 0.3	V
V_{IL}	LOW-level input voltage	LVCMOS		−0.3	-	+0.7	V
$V_{i(p-p)}$	peak-to-peak input voltage	PCLK; LVPECL		250	-	-	V
V_{ICR}	common mode input voltage range	PCLK; LVPECL	[1]	1.1	-	V_{CC} − 0.7	V
I_I	input current	V_I = GND or V_I = V_{CC}	[2]	-	-	±200	µA
V_{OH}	HIGH-level output voltage	I_{OH} = −15 mA	[3]	1.8	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 15 mA	[2]	-	-	0.6	V
Z_o	output impedance			-	17 to 20	-	Ω
$I_{CC(max)}$	maximum supply current	all V_{CC} pins	[4]	-	-	2.0	mA

[1] V_{ICR} (DC) is the crossing point of the differential input signal. Functional operation is obtained when the crossing point is within the V_{ICR} range and the input swing lies within the $V_{i(p-p)}$ (DC) specification.

[2] Input pull-up/pull-down resistors influence input current.

[3] The PCK9456 is capable of driving 50 Ω transmission lines on the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of V_T. Alternatively, the device drives up to two 50 Ω series terminated transmission lines.

[4] $I_{CC(max)}$ is the DC current consumption of the device with all outputs open and the input in its default state or open.

Table 10. Dynamic characteristics (3.3 V)

T_{amb} = −40 °C to +85 °C; V_{CC} = $V_{CC(bankA)}$ = $V_{CC(bankB)}$ = $V_{CC(bankC)}$ = 3.3 V ± 5 %[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_i	input frequency		[2]	0	-	250	MHz
$f_{o(max)}$	maximum output frequency	divide-by-1 output; FSELx = 0	[2]	0	-	250	MHz
		divide-by-2 output; FSELx = 1		0	-	125	MHz
$V_{i(p-p)}$	peak-to-peak input voltage	PCLK; LVPECL		500	-	1000	mV
V_{ICR}[3]	common mode input voltage range	PCLK; LVPECL		1.3	-	V_{CC} − 0.8	V
$t_{p(i)(ref)}$	reference input pulse duration			1.4	-	-	ns
t_r	rise time	PCLK input; 0.8 V to 2.0 V		-	-	1.0[4]	ns
t_f	fall time	PCLK input; 2.0 V to 0.8 V		-	-	1.0[4]	ns
t_{PLH}	LOW-to-HIGH propagation delay	CCLK to any Q		2.2	2.8	4.45	ns
t_{PHL}	HIGH-to-LOW propagation delay	CCLK to any Q		2.2	2.8	4.2	ns
t_{PLZ}	LOW to OFF-state propagation delay[5]			-	-	10	ns
t_{PHZ}	HIGH to OFF-state propagation delay[5]			-	-	10	ns
t_{PZL}	OFF-state to LOW propagation delay[6]			-	-	10	ns
t_{PZH}	OFF-state to HIGH propagation delay[6]			-	-	10	ns
$t_{sk(o)}$	output skew time	output-to-output					
		within one bank		-	-	150	ps
		any output bank, same output divider		-	-	200	ps
		any output, any output divider		-	-	1.0	ns
$t_{sk(pr)}$	process skew time	part-to-part		-	-	1.0	ns
$t_{sk(p)}$	pulse skew time	output	[7]	-	-	500	ps
δ_o	output duty cycle	divide-by-1 output; δ_{ref} = 50 %		47	50	62.5	%
		divide-by-2 output; δ_{ref} = 25 % to 75 %		45	50	55	%
t_r	rise time	output; 0.55 V to 2.4 V		0.2	-	1.0	ns
t_f	fall time	output; 2.4 V to 0.55 V		0.2	-	1.0	ns

[1] Dynamic (AC) characteristics apply for parallel output termination of 50 Ω to V_T.

[2] The PCK9456 is functional up to an input and output clock frequency of 350 MHz and is characterized up to 250 MHz.

[3] V_{ICR} (AC) is the crossing point of the differential input signal. Normal AC operation is obtained when the crossing point is within the V_{ICR} range and the input swing lies within the $V_{i(p-p)}$ (AC) specification.

[4] Violation of the 1.0 ns maximum input rise and fall time limit will affect the device propagation delay, part-to-part skew, reference input pulse width, output duty cycle and maximum frequency specifications.

[5] Output disable time.

[6] Output enable time.

[7] Output pulse skew is the absolute difference of the propagation delay times: $|t_{PLH} - t_{PHL}|$.

Table 11. Dynamic characteristics (2.5 V)

T_{amb} = −40 °C to +85 °C; V_{CC} = $V_{CC(bankA)}$ = $V_{CC(bankB)}$ = $V_{CC(bankC)}$ = 2.5 V ± 5 %[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_i	input frequency		[2]	0	-	250	MHz
$f_{o(max)}$	maximum output frequency	divide-by-1 output; FSELx = 0	[2]	0	-	250	MHz
		divide-by-2 output; FSELx = 1		0	-	125	MHz
$V_{i(p-p)}$	peak-to-peak input voltage	PCLK; LVPECL		500	-	1000	mV
V_{ICR}[3]	common mode input voltage range	PCLK; LVPECL		1.1	-	V_{CC} − 0.7	V
$t_{p(i)(ref)}$	reference input pulse duration			1.4	-	-	ns
t_r	rise time	PCLK input; 0.7 V to 1.7 V		-	-	1.0[4]	ns
t_f	fall time	PCLK input; 1.7 V to 0.7 V		-	-	1.0[4]	ns
t_{PLH}	LOW-to-HIGH propagation delay	PCLK to any Q		2.6	-	5.6	ns
t_{PHL}	HIGH-to-LOW propagation delay	PCLK to any Q		2.6	-	5.5	ns
t_{PLZ}	LOW to OFF-state propagation delay[5]			-	-	10	ns
t_{PHZ}	HIGH to OFF-state propagation delay[5]			-	-	10	ns
t_{PZL}	OFF-state to LOW propagation delay[6]			-	-	10	ns
t_{PZH}	OFF-state to HIGH propagation delay[6]			-	-	10	ns
$t_{sk(o)}$	output skew time	output-to-output					
		within one bank		-	-	150	ps
		any output bank, same output divider		-	-	200	ps
		any output, any output divider		-	-	1.0	ns
$t_{sk(pr)}$	process skew time	part-to-part		-	-	3.0	ns
$t_{sk(p)}$	pulse skew time	output	[7]	-	-	500	ps
δ_o	output duty cycle	divide-by-1 or divide-by-2 output; δ_{ref} = 50 %		45	50	62.5	%
t_r	rise time	output; 0.6 V to 1.8 V		0.1	-	1.0	ns
t_f	fall time	output; 1.8 V to 0.6 V		0.1	-	1.0	ns

[1] Dynamic (AC) characteristics apply for parallel output termination of 50 Ω to V_T.

[2] The PCK9456 is functional up to an input and output clock frequency of 350 MHz and is characterized up to 250 MHz.

[3] V_{ICR} (AC) is the crossing point of the differential input signal. Normal AC operation is obtained when the crossing point is within the V_{ICR} range and the input swing lies within the $V_{i(p-p)}$ (AC) specification.

[4] Violation of the 1.0 ns maximum input rise and fall time limit will affect the device propagation delay, part-to-part skew, reference input pulse width, output duty cycle and maximum frequency specifications.

[5] Output disable time.

[6] Output enable time.

[7] Output pulse skew is the absolute difference of the propagation delay times: $|t_{PLH} - t_{PHL}|$.

Table 12. Dynamic characteristics

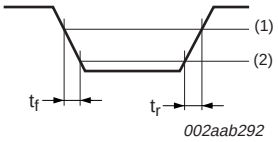
T_{amb} = −40 °C to +85 °C; V_{CC} = 3.3 V ± 5 %; $V_{CC(bankA)}$ = $V_{CC(bankB)}$ = $V_{CC(bankC)}$ = 2.5 V ± 5 % or 3.3 V ± 5 %[1][2]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{sk(o)}$	output skew time	output-to-output				
		within one bank	-	-	150	ps
		any output bank, same output divider	-	-	250	ps
		any output, any output divider	-	-	350	ps
$t_{sk(pr)}$	process skew time	part-to-part	-	-	2.5	ns
$t_{sk(p)}$	pulse skew time	output [3]	-	-	250	ps
t_{PLH}	LOW-to-HIGH propagation delay	PCLK to any Q	see Table 10			
t_{PHL}	HIGH-to-LOW propagation delay	PCLK to any Q	see Table 10			
δ_o	output duty cycle	δ_{ref} = 50 %	45	50	55	%

[1] Dynamic (AC) characteristics apply for parallel output termination of 50 Ω to V_T.

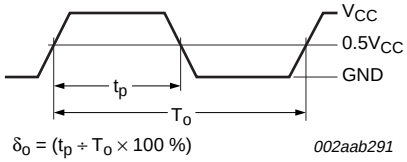
[2] For all other dynamic (AC) specifications, refer to 2.5 V or 3.3 V tables according to the supply voltage of the output bank.

[3] Output pulse skew is the absolute difference of the propagation delay times: $|t_{PLH} - t_{PHL}|$.



(1) 2.4 V (V_{CC} = 3.3 V)
1.8 V (V_{CC} = 2.5 V)
(2) 0.55 V (V_{CC} = 3.3 V)
0.6 V (V_{CC} = 2.5 V)

Fig 3. Output transition time test reference



The time from the PLL controlled edge to the non-controlled edge, divided by the time between PLL controlled edges, expressed as a percentage.

Fig 4. Output duty cycle (δ_o)

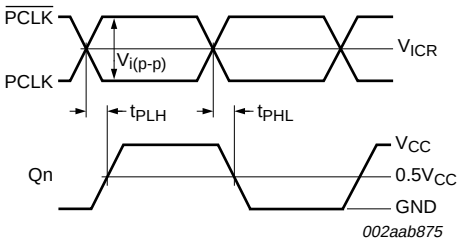
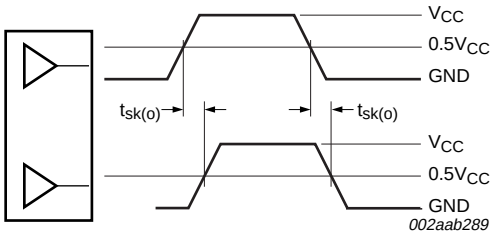


Fig 5. Propagation delay (t_{PD}) test reference



The pin-to-pin skew is defined as the worst-case difference in propagation delay between any similar delay path within a single device.

Fig 6. Output-to-output skew ($t_{sk(o)}$)

10. Application information

10.1 Driving transmission lines

The PCK9456 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user, the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20 Ω, the drivers can drive either parallel or series terminated transmission lines.

In most high performance clock networks, point-to-point distribution of signals is the method of choice. In a point-to-point scheme, either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50 Ω resistance to $0.5V_{CC}$. This technique draws a fairly high level of DC current, and thus only a single terminated line can be driven by each output of the PCK9456 clock driver. For the series terminated case, however, there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 7 illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme, the fan-out of the PCK9456 clock driver is effectively doubled due to its capability to drive multiple lines.

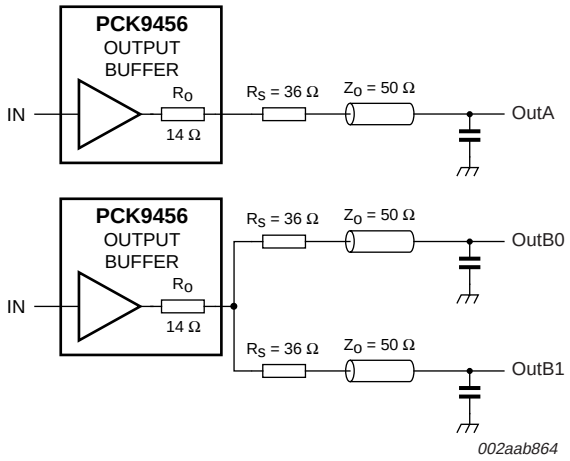


Fig 7. Single versus dual transmission lines

The waveform plots of Figure 8 show simulation results of an output driving a single line versus two lines. In both cases the drive capability of the PCK9456 output buffer is more than sufficient to drive 50 Ω transmission lines on the incident edge. Note from the delay measurement in the simulations a delta of only 43 ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the PCK9456. The output waveform in Figure 8 shows a step in the waveform; this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36 Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S\left(\frac{Z_o}{R_s + R_o + Z_o}\right)$$

where:

Z_o = 50 Ω || 50 Ω

R_s = 36 Ω || 36 Ω

R_o = 14 Ω

$$V_L = 3.0\left(\frac{25}{18 + 14 + 25}\right) = 1.31\ V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.5 V. It will then increment towards the quiescent 3.0 V in steps separated by one round trip delay (in this case 4.0 ns).

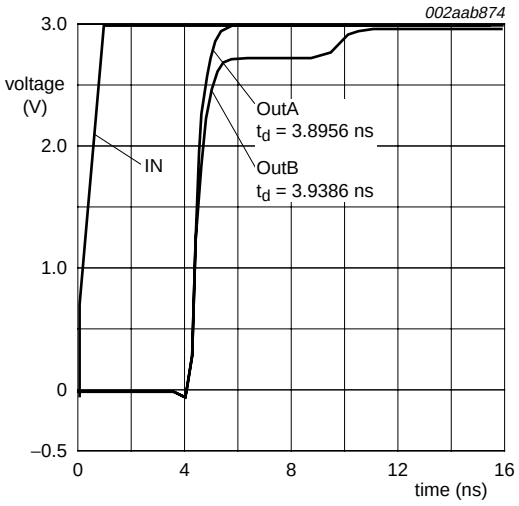
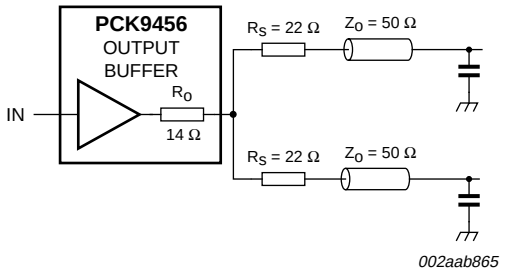


Fig 8. Single versus dual line termination waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines, the situation in Figure 9 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



14 Ω + 22 Ω || 22 Ω = 50 Ω || 50 Ω

25 Ω = 25 Ω

Fig 9. Optimized dual line termination

11. Test information

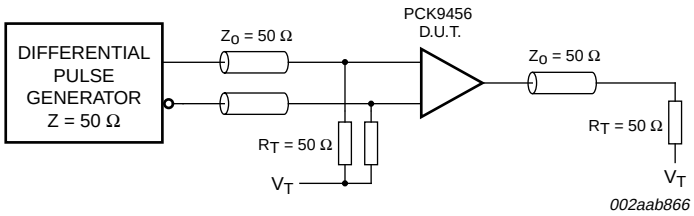
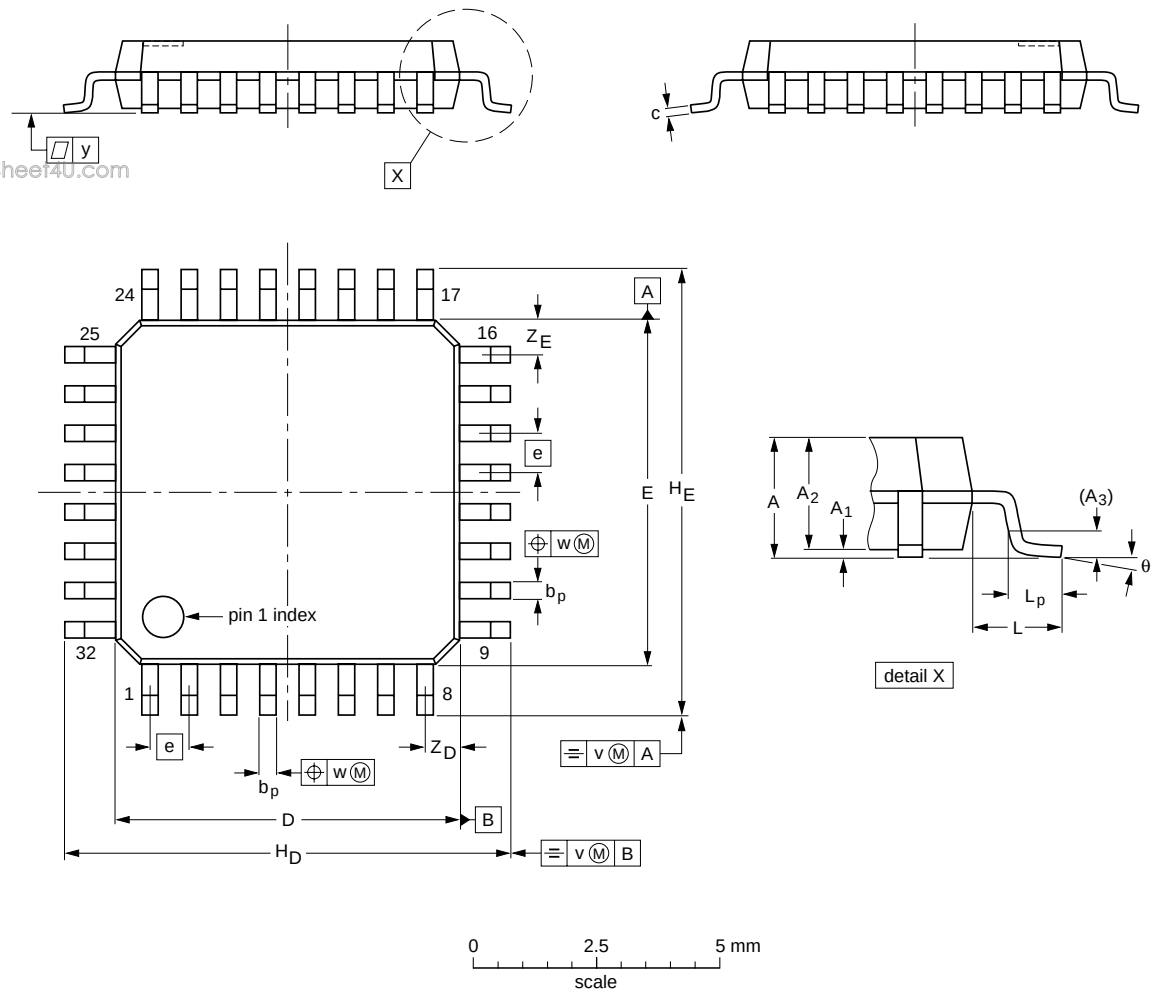


Fig 10. PCLK PCK9456 AC test reference for V_{CC} = 3.3 V and V_{CC} = 2.5 V

12. Package outline

LQFP32: plastic low profile quad flat package; 32 leads; body 7 x 7 x 1.4 mm **SOT358-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.4 0.3	0.18 0.12	7.1 6.9	7.1 6.9	0.8	9.15 8.85	9.15 8.85	1	0.75 0.45	0.2	0.25	0.1	0.9 0.5	0.9 0.5	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT358 -1	136E03	MS-026				~~03-02-25~~ 05-11-09

Fig 11. Package outline SOT358-1 (LQFP32)

13. Soldering

13.1 Introduction to soldering surface mount packages

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

13.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow temperatures range from 215 °C to 260 °C depending on solder paste material. The peak top-surface temperature of the packages should be kept below:

Table 13. SnPb eutectic process - package peak reflow temperatures (from *J-STD-020C* July 2004)

Package thickness	Volume mm^3 < 350	Volume mm^3 ≥ 350
< 2.5 mm	240 °C + 0/–5 °C	225 °C + 0/–5 °C
≥ 2.5 mm	225 °C + 0/–5 °C	225 °C + 0/–5 °C

Table 14. Pb-free process - package peak reflow temperatures (from *J-STD-020C* July 2004)

Package thickness	Volume mm^3 < 350	Volume mm^3 350 to 2000	Volume mm^3 > 2000
< 1.6 mm	260 °C + 0 °C	260 °C + 0 °C	260 °C + 0 °C
1.6 mm to 2.5 mm	260 °C + 0 °C	250 °C + 0 °C	245 °C + 0 °C
≥ 2.5 mm	250 °C + 0 °C	245 °C + 0 °C	245 °C + 0 °C

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

13.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):

- larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
- smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

13.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

13.5 Package related soldering information

Table 15. Suitability of surface mount IC packages for wave and reflow soldering methods

Package[1]	Soldering method	
	Wave	Reflow[2]
BGA, HTSSON..T[3], LBGA, LFBGA, SQFP, SSOP..T[3], TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[4]	suitable
PLCC[5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[5][6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended[7]	suitable
CWQCCN..L[8], PMFP[9], WQCCN..L[8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

[9] Hot bar soldering or manual soldering is suitable for PMFP packages.

14. Abbreviations

Table 16. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
HBM	Human Body Model
LVCMOS	Low Voltage Complementary Metal Oxide Semiconductor
LVPECL	Low Voltage Positive Emitter Coupled Logic
MM	Machine Model
PECL	Positive Emitter Coupled Logic

15. Revision history

Table 17. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCK9456_1	20060731	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.semiconductors.philips.com.

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