DATA SHEET

ARIZONA MICROTEK, INC.

AZ10E111
AZ100E111

1:9 Differential Clock Driver

FEATURES

- Low Skew
- Guaranteed Skew Spec
- Differential Design
- Enable
- V_{BB} Output
- Extended 100E V_{EE} Range of -4.2V to -5.46V
- 75kΩ Internal Input Pulldown Resistors
- Direct Replacement for Motorola MC10EL111 & MC100EL111
- Manufactured Under License By Lucent Technologies

PACKAGE AVAILABILITY

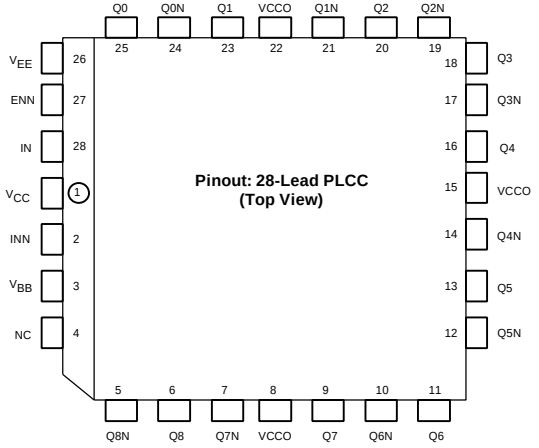
SUFFIX	DESCRIPTION
FN	Plastic 28 PLCC

DESCRIPTION

The AZ10E/100E111 is a low skew 1-to-9 differential driver, designed with clock distribution in mind. It accepts one signal input, which can be either differential or single-ended if the VBB output is used. The signal is fanned-out to 9 identical differential outputs. An Enable input is also provided. A HIGH disables the device by forcing all Q outputs LOW and all QN outputs HIGH.

The device is specifically designed, modeled and produced with low skew as the key goal. Optimal design and layout serve to minimize gate-to-gate skew within-device, and empirical modeling is used to determine process control limits that ensure consistent t_{pd} distributions from lot-to-lot. The net result is a dependable, guaranteed low skew device.

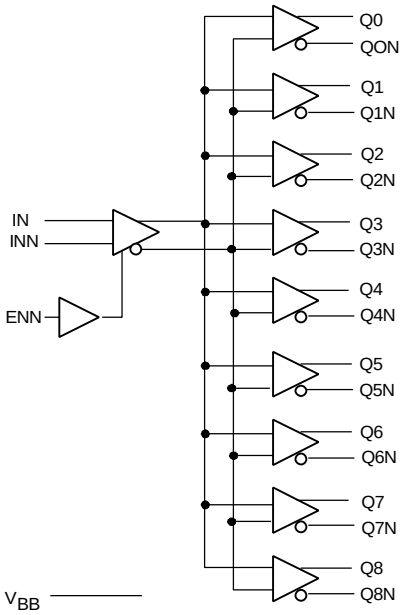
To ensure that the tight skew specification is met, both sides of the differential output must be terminated into 50Ω, even if only one side is used. In most applications all nine differential pairs will be used and therefore terminated. In the case where fewer than nine pairs are used, it is necessary to terminate at least the output pairs on the same package side (i.e. sharing the same V_{CCO}) as the pair(s) being used on that side, in order to maintain minimum skew. Failure to do this will result in small degradations of propagation delay (on the order of 10-20ps) of the output(s) being used which, while not being catastrophic to most designs, will mean a loss of skew margin.



PIN DESCRIPTION

PIN	FUNCTION
IN, INN	Differential Input Pair
ENN	Enable
Q_0, Q_0N-Q_8N, Q_8	Differential Outputs V_{BB} Output

LOGIC SYMBOL



AZ10E111
AZ100E111

DC Characteristics (V_{EE} = 10E(-4.94V to -5.46V),100E(-4.2V to -5.46V); V_{CC} = V_{CCO} = GND)

		-40 ℃			0 ℃			25 ℃			85 ℃				
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Cond**
V_{BB}	Reference Voltage 10E	-1.43		-1.30	-1.38		-1.27	-1.35		-1.25	-1.31		-1.19	V	
	100E	-1.38		-1.26	-1.38		-1.26	-1.38		-1.26	-1.38		-1.26		
I_{IH}	Input HIGH Current			150			150			150			150	µA	
I_{EE}	Power Supply 10E		48	60		48	60		48	60		48	60	mA	
	Current 100E		48	60		48	60		48	60		55	69		
V_{PP} (DC)	Input Sensitivity	50			50			50			50			mV	1
V_{CMR}	Common Mode Range	-1.6		-0.4	-1.6		-0.4	-1.6		-0.4	-1.6		-0.4	V	2

1. Differential input voltage required to obtain a full ECL swing on the outputs.
2. V_{CMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The V_{IL} level must be such that the peak-to-peak voltage is less than 1.0V and greater than or equal to V_{PP}(min).

AC Characteristics (V_{EE} = 10E(-4.94V to -5.46V),100E(-4.2V to -5.46V); V_{CC} = V_{CCO} = GND)

		-40 ℃			0 ℃			25 ℃			85 ℃				
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Cond**
	Propagation Delay														
t_{PLH}	to Output IN (Diff)	380		680	460		560	480		580	510		610		1
t_{PHL}	IN (SE)	280		780	410		610	430		630	460		660	ps	2
	Enable	400		900	450		850	450		850	450		850		3
	Disable	400		900	450		850	450		850	450		850		3
t_S	Setup Time ENN to IN	250	0		200	0		200	0		200	0		ps	5
t_h	Hold Time IN to ENN	50	-200		0	-200		0	-200		0	-200		ps	6
t_R	Release Time ENN to IN	350	100		300	100		300	100		300	100		ps	7
t_{skew}	Within-Device Skew		25	75		25	50		25	50		25	50	ps	4
V_{PP} (AC)	Minimum Input Swing	250			250			250			250			mV	8
t_r / t_f	Rise/Fall Time	250	450	650	275	375	600	275	375	600	275	375	600	ps	

1. The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals.
2. The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal.
3. Enable is defined as the propagation delay from the 50% point of a **negative** transition on ENN to the 50% point of a **positive** transition on Q (or a negative transition on QN). Disable is defined as the propagation delay from the 50% point of a **positive** transition on ENN to the 50% point of a **negative** transition on Q (or a positive transition on QN).
4. The within-device skew is defined as the worst case difference between any two similar delay paths within a single device.
5. The setup time is the minimum time that ENN must be asserted prior to the next transition of IN/INN to prevent an output response greater than ±75 mV to that IN/INN transition (see Figure 1).
6. The hold time is the minimum time that ENN must remain asserted after a negative going IN or a positive going INN to prevent an output response greater than ±75 mV to that IN/INN transition (see Figure 2).
7. The release time is the minimum time that ENN must be deasserted prior to the next IN/INN transition to ensure an output response that meets the specified IN to Q propagation delay and output transition times (see Figure 3).
8. V_{PP}(min) is defined as the minimum input differential voltage which will cause no increase in the propagation delay. The V_{PP}(min) is AC limited for the E111, as a differential input as low as 50 mV will still produce full ECL levels at the output.

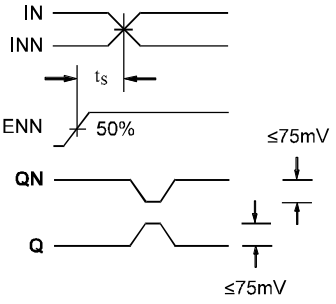


Figure 1. Setup Time

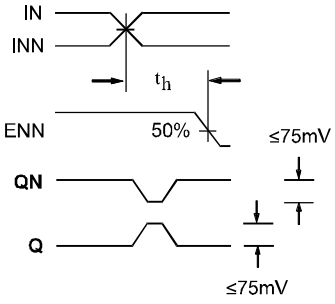


Figure 2. Hold Time

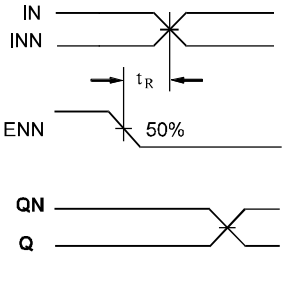


Figure 3. Release Time