PLL FREQUENCY SYNTHESIZER

The integrated circuit SAA1056P together with a suitable prescaler (e.g. SAA1059) and a loop filter forms a complete PLL frequency synthesizer for AM/FM radio tuning systems.

Features

- Bus control for the selection of 17-bit words.
- 17-bit latch, for data storage.
- Control lines TTL compatible by means of level shifters.
- Decoupled oscillator frequency output (system clock for other ICs).
- Choice of 4 reference frequencies.

QUICK REFERENCE DATA

Supply voltage ranges	V_{DD}	8 to 10 V
	V_{DDI}	4,5 to 5,5 V
Operating ambient temperature range	T_{amb}	−20 to + 80 °C
Maximum input frequency	f_I	4 MHz

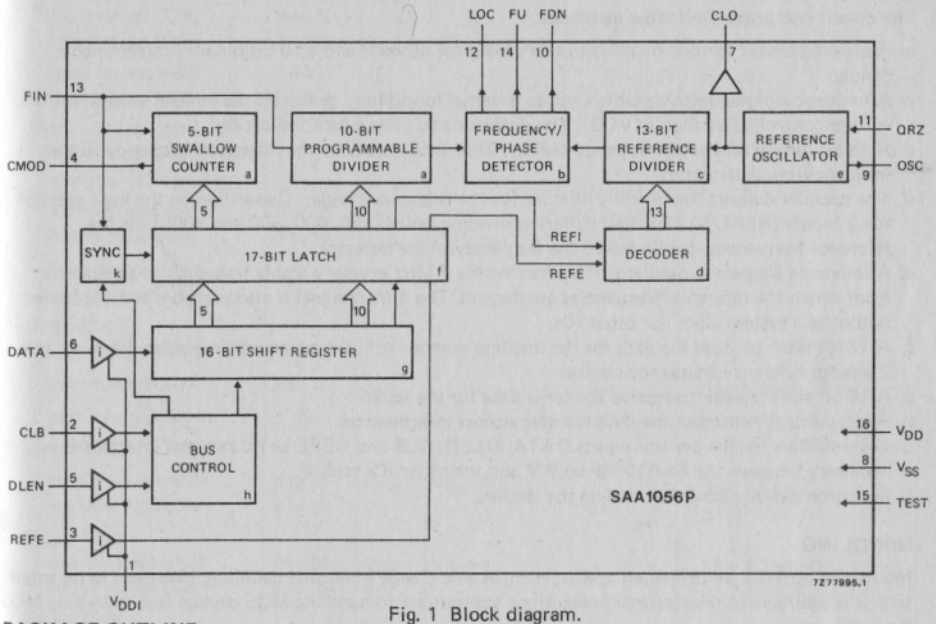


Fig. 1 Block diagram.

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38Z).

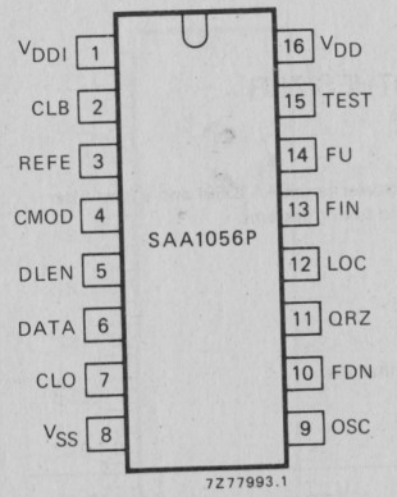


Fig. 2 Pinning diagram.

PINNING

16	V_{DD}	positive supply
8	V_{SS}	ground (0 V)
1	V_{DDI}	supply voltage for the level shifters

Inputs

13	FIN	input frequency; maximum 4 MHz	
6	DATA	data input	CBUS
2	CLB	clock burst	CBUS
5	DLEN	data line enable	CBUS
3	REFE	reference frequency selection	
11	QRZ	quartz crystal input (4 MHz)	

Outputs

4	CMOD	count mode output for prescaler
12	LOC	lock detector output
10	FDN	phase detector output; frequency down
14	FU	phase detector output; frequency up
7	CLO	system clock for other ICs (4 MHz)
9	OSC	quartz crystal oscillator output

GENERAL DESCRIPTION

The integrated circuit SAA1056P, together with a suitable prescaler (32/33) and loop-filter, forms a complete synthesizer function for AM/FM radio tuning systems.

The circuit comprises the following blocks:

a. A dividing circuit formed by a 5-bit binary Swallow counter and a 10-bit binary programmable divider.
b. A frequency/phase detector which, via an external loop-filter, generates the control voltage for the voltage-controlled oscillator (VCO). The detector also gives a lock indication.
c. A 13-bit binary reference frequency divider. This divider delivers the reference frequency to the frequency/phase detector.
d. The decoder delivers the dividing number for the reference divider. Depending on the logic state of the 2 inputs (REFI, REFE), four different dividing ratios (160, 400, 800 and 8000) for the reference frequencies can be fed to the frequency/phase detector.
e. A reference frequency oscillator. Together with a 4 MHz crystal a stable frequency is generated, from which the reference frequencies are derived. The 4 MHz signal is also available at a decoupled output as a system clock for other ICs.
f. A 17-bit latch to store the data for the dividing number of the programmable divider (block a) and 2 bits for reference frequency choice.
g. A 16-bit shift register to receive the serial data for the latch.
h. A bus control to protect the data transfer against interferences.
i. Level shifters for the control inputs DATA, DLEN, CLB and REFE so no external interface is necessary between the SAA1056P on 9 V and the other ICs on 5 V.
k. Synchronization circuit for loading the latches.

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range ($V_{DDI} < V_{DD}$)	V_{DD}		−0,3 to + 15	V
Input voltage range	V_I		−0,3 to + V_{DD}	V
Input current (d.c.)	$\pm I_I$	max.	10	mA
Output current (d.c.)	$\pm I_O$	max.	10	mA
Current from V_{DDI} to V_{DD} (d.c.)	I	max.	10	mA
Power dissipation per output	P_O	max.	100	mW
Total power dissipation per package	P_{tot}	max.	240	mW
Operating ambient temperature range	T_{amb}		−20 to + 80	°C
Storage temperature range	T_{stg}		−55 to + 150	°C

D.C. CHARACTERISTICS

V_{SS} = 0; T_{amb} = −20 to + 80 °C; unless otherwise specified

	V_{DD} V	symbol	min.	typ.	max.		conditions
Supply voltages	–	V_{DD}	8	9	10	V	
	–	V_{DDI}	4,5	5	5,5	V	
Supply current	10	I_{DD}	–	–	100	μA	I_O = 0; V_I = V_{DD} or V_{DDI} or V_{SS}
Inputs without level shifters; FIN, QRZ, TEST							
input voltage LOW	8 to 10	V_{IL}	0	–	0,3 V_{DD}	V	
input voltage HIGH	8 to 10	V_{IH}	0,7 V_{DD}	–	V_{DD}	V	
input current HIGH	10	I_{IH}	–	–	1	μA	V_I = 10 V
input current LOW	10	$-I_{IL}$	–	–	1	μA	V_I = 0
Inputs with level shifters DATA, CLB, DLEN, REFE at V_{DDI} = 4,5 to 5,5 V							
input voltage LOW	8 to 10	V_{IL}	0	–	0,2 V_{DDI}	V	
input voltage HIGH	8 to 10	V_{IH}	0,8 V_{DDI}	–	V_{DDI}	V	
input current HIGH	10	I_{IH}	–	–	1	μA	V_I = V_{DDI}
input current LOW	10	$-I_{IL}$	–	–	1	μA	V_I = 0
Output CMOD open-drain, n-channel							
output voltage LOW	8 to 10	V_{OL}	–	–	0,5	V	I_{OL} = 5,5 mA
output leakage current	10	I_{OR}	–	–	20	μA	V_O = 10 V
Outputs LOC, FU, FDN							
output voltage HIGH	8 to 10	V_{OH}	V_{DD}−0,5	–	–	V	$-I_O$ = 2,5 mA
output voltage LOW	8 to 10	V_{OL}	–	–	0,5	V	I_O = 5,5 mA
Output OSC							
output voltage HIGH	8 to 10	V_{OH}	V_{DD}−1	–	–	V	$-I_O$ = 1,2 mA; QRZ at V_{SS}
output voltage LOW	8 to 10	V_{OL}	–	–	1	V	I_O = 2 mA; QRZ at V_{DD}
Output CLO							
output voltage HIGH	8 to 10	V_{OH}	V_{DD}−1	–	–	V	$-I_O$ = 1,2 mA
output voltage LOW	8 to 10	V_{OL}	–	–	1	V	I_O = 4 mA

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = −20 to + 80 °C; unless otherwise specified

	V_{DD} V	symbol	min.	typ.	max.	conditions
Inputs without level shifters; FIN, QRZ						
input frequency	8 to 10	f_i	4	–	– MHz	
duty factor	8 to 10	δ	45	–	55 %	
rise/fall time	8 to 10	t_r, t_f	–	–	50 ns	
Inputs with level shifter DATA, CLB, DLEN, REFE						
rise/fall time	8 to 10	t_r, t_f	–	–	1 µs	at 0,8 × V_{DD} resp. 0,2 × V_{DD} levels
pulse width	–	t_{WH}, t_{WL}	500	–	– ns	
Output CMOD open-drain, n-channel						
fall time	8 to 10	t_f	–	–	20 ns	C_L = 25 pF, R_L = 1,2 kΩ ± 20%
Output CLO						
pulse period	8 to 10	T	250	–	– ns	see Figs 3 and 4
pulse width HIGH	–	t_{WH}	90	–	– ns	
pulse width LOW	–	t_{WL}	90	–	– ns	
Output LOC, FU, FDN rise/fall time	8 to 10	t_r, t_f	–	–	20 ns	C_L = 25 pF, R_L = 10 kΩ ± 10%

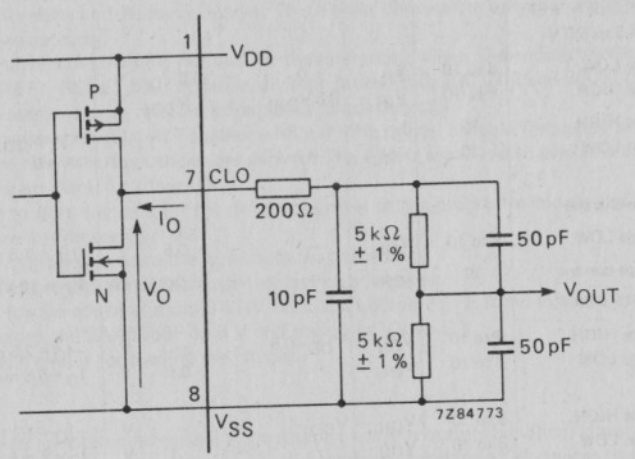


Fig. 3 Output CLO test circuit.

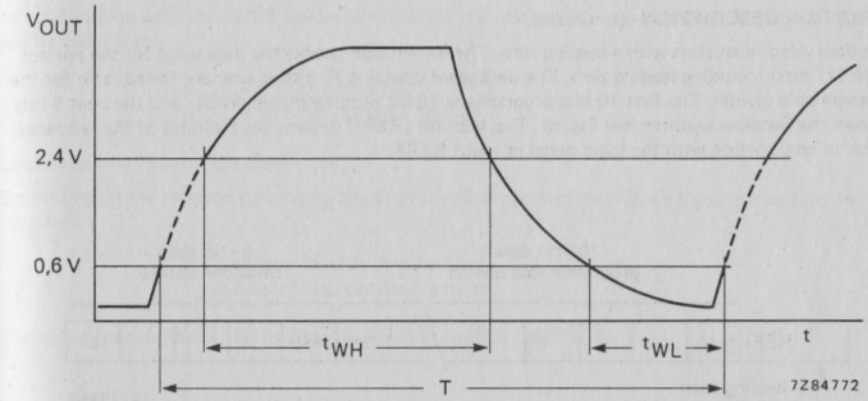


Fig. 4 Output voltage (V_{OUT}) of Fig. 3 as a function of time.

OPERATION DESCRIPTION

Data **inputs** (DLEN and DATA)

The SAA1056P accepts the serial 17-bit data word synchronized with the clock burst (CLB), are offered at the data input DATA. However, a command is accepted only when the data line enable input DLEN is HIGH at the same time.

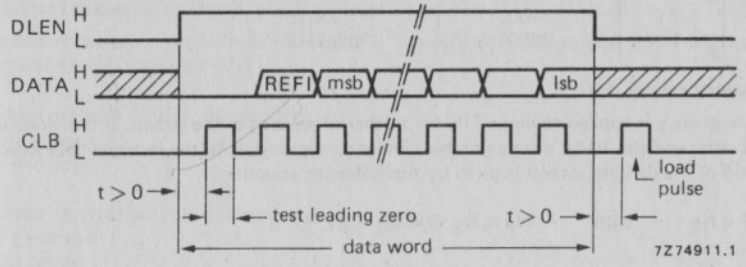


Fig. 5 Pulse diagram of the 17-bit data word.

OPERATION DESCRIPTION (continued)

Each data word must start with a leading zero. The SAA1056P checks the data word for the correct length (17 bits) including leading zero. The data word contains 15 bits as a binary coded ratio for the programmable divider. The first 10 bits program the 10-bit programmable divider and the next 5 bits program the Swallow counter (see Fig. 6). The 16th bit (REFI) determines the ratio of the reference divider in conjunction with the logic signal at input REFE.

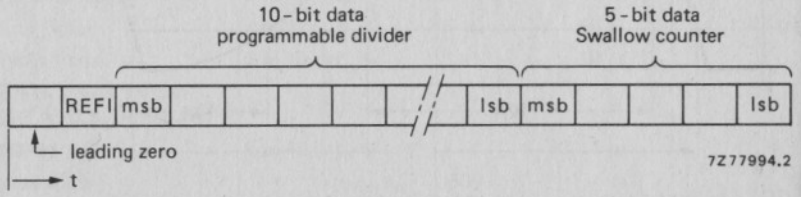


Fig. 6 Organization of a data word.

Setting the reference divider (input REFE and control-bit REFI)

The reference divider can be set to four different ratios, using the two signals REFE and REFI.

control bit REFI	input REFE	dividing ratio N_{ref}	reference frequency at f_{osc} = 4 MHz; f_{ref}
1	1	160	25 kHz
1	0	400	10 kHz
0	1	800	5 kHz
0	0	8000	0,5 kHz

Input frequency divider (FIN)

The input frequency is applied to input FIN for further processing in the circuit. It is divided in the Swallow counter and the 10-bit programmable divider corresponding to the received data word. The division ratio of the dividing circuit is given by the following equation:

$N = N_S + P \times N_P$ with: $N_P \leqslant N_S; 0 \leqslant N_S \leqslant 31$

in which:

N = division ratio of total divider
N_S = value for the Swallow counter
P = lowest division ratio of prescaler
N_P = division ratio of the 10-bit programmable divider.

In combination with the 32/33 divider (SAA1059), the minimum and maximum dividing number can be calculated:

$N_{min} = 0 + 32 \times 31 = 992$
$N_{max} = 31 + 32 \times 1023 = 32\,767$

Count mode output for prescaler (CMOD)

Depending on the received data word, the 5-bit Swallow counter generates a signal for setting the prescaler.

0 = divide by low dividing number
1 = divide by high dividing number.

The signal appears about 150 ns after the input pulse FIN (see Fig. 7).

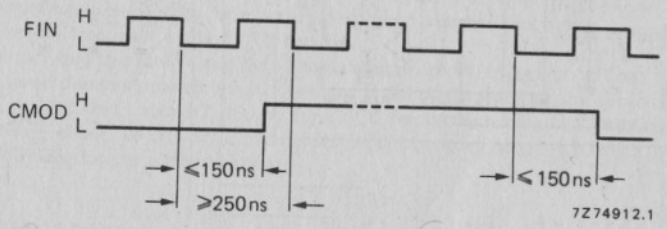


Fig. 7 Timing of the CMOD signal.

Phase detector (frequency up/down) and lock detector outputs (FDN, FU, LOC)

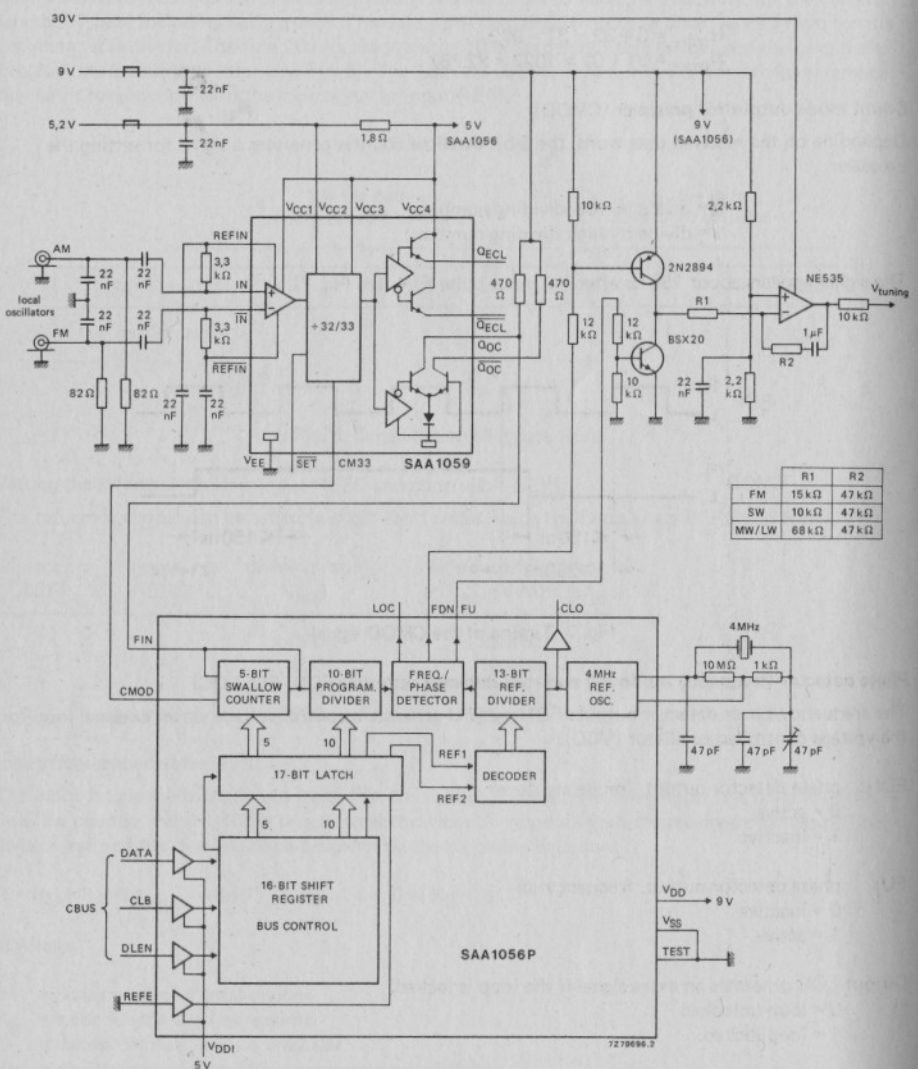
The frequency/phase detector outputs FDN and FU generate a control voltage via an external loop for the voltage-controlled oscillator (VCO).

FDN: phase detector output, frequency down
0 = active
1 = inactive

FU: phase detector output, frequency up
0 = inactive
1 = active

Output LOC generates an extra signal if the loop is locked.
0 = loop unlocked
1 = loop locked.

APPLICATION INFORMATION



	R1	R2
FM	15 kΩ	47 kΩ
SW	10 kΩ	47 kΩ
MW/LW	68 kΩ	47 kΩ

Fig. 8 A practical digital frequency synthesizer for a radio receiver.