

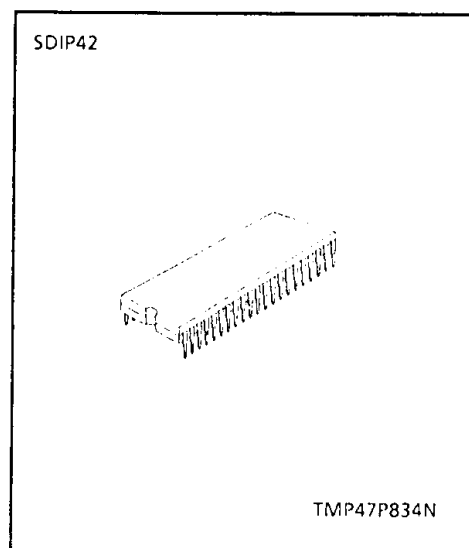
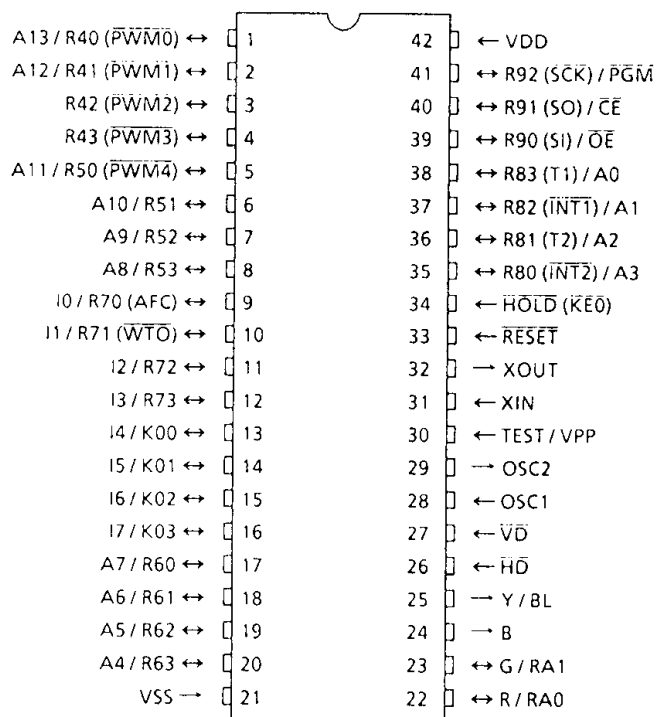
CMOS 4-BIT MICROCONTROLLER

TMP47P834N

The 47P834 is the OTP microcontroller with 64kbits PROM. For program operation, the programming is achieved by using with EPROM programmer (TMM27128A type) and adaptor socket. The function of this device is exactly same as the 47C834.

PART No.	ROM	RAM	PACKAGE
TMP47P834N	OTP 8192 x 8-bit	512 x 4-bit	SDIP42

PIN ASSIGNMENT (TOP VIEW)



PIN FUNCTION

The 47P834 has MCU mode and PROM mode.

(1) MCU mode

The 47C834 and the 47P834 are pin compatible (TEST pin for out-going test. Be fixed to low level).

(2) PROM mode

PIN NAME	Input / Output	FUNCTIONS	PIN NAME (MCU mode)
A13 - A12	Input	Address inputs	R41 - R40
A11 - A8			R53 - R50
A7 - A4			R63 - R60
A3 - A0			R83 - R80
I7 - I4	I/O	Data Inputs / outputs	K03 - K00
I3 - I0			R73 - R70
PGM	Input	Program control input	R92
\overline{CE}		Chip Enable input	R91
\overline{OE}		Output Enable input	R90
VPP	Power supply	+ 12.5V / 5V (Program supply voltage)	TEST
VCC		+ 5V	VDD
VSS		0V	VSS
OSC1	Output	OSD resonator connecting pins	
OSC2			
Y, B, \overline{HD} , \overline{VD}	OSD output	Be fixed to low level	
G / R			
\overline{RESET}	Input	PROM mode setting pin. Be fixed to low level.	
\overline{HOLD}	Input		
XIN	Input	Resonator connecting pins	
XOUT	Output		

OPERATIONAL DESCRIPTION

The following is an explanation of hardware configuration and operation in relation to the 47P834. The 47P834 is the same as the 47C834 except that an EPROM or OTP is used instead of a built-in mask ROM.

1. OPERATION mode

The 47P834 has an MCU mode and a PROM mode.

1.1 MCU mode

The MCU mode is set by fixing the TEST/VPP pin at the "L" level. Operation in the MCU mode is the same as for the 47C834, except that the TEST/VPP pin does not have built in pull-down resistor and cannot be used open.

1.1.1 Program Memory

The program storage area is the same as for the 47C834. Data conversion tables must be set in two locations when using the 47P834 to check 47C434/634 operation.

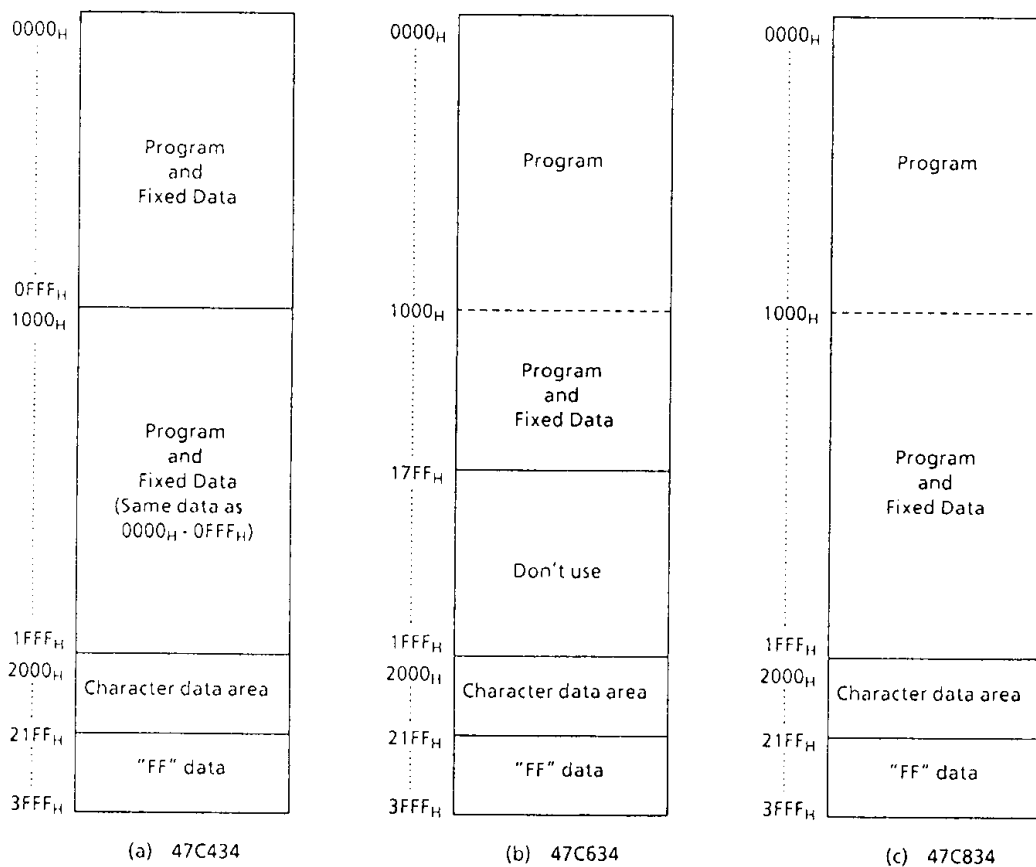


Figure 1-1. Program area

1.1.2 Data Memory

The 47P834 has two built-in 256 × 4-bit data memory banks (DMB0, DMB1).

When using the 47P834 as a 47C634 evaluator, do not write data to address 80H and following, even though the DMB1 addresses are 00-FFH. And when using as a 47C434 evaluator, do not write data to the whole DMB1. There is no necessary to take into consideration a special function shared area, because one is built in DMB0.

1.1.3 Other Peripheral Hardware Function

Using as 47C434/634 evaluator, do not write data into the command register OP0B of PULSE output control and Image Receiving Mode Control.

1.1.4 Input/Output Circuitry

(1) Control pins

This is the same as for the 47C434/634/834 except that there is no built in pull-down resistor for the TEST pin. Input/output circuitry of the 47P834 control pins is shown below.

CONTROL PIN	I/O	CIRCUITRY	REMARKS
XIN XOUT	Input Output		Resonator connecting pins $R = 1K\Omega$ (typ.) $R_f = 1.5M\Omega$ (typ.) $R_O = 2K\Omega$ (typ.)
RESET	Input		Hysteresis input Contained pull-up resistor $R_{IN} = 220K\Omega$ (typ.) $R = 1K\Omega$ (typ.)
HOLD ($\overline{KE0}$)	Input (Input)		Hysteresis input (Sense input) $R = 1K\Omega$ (typ.)
TEST	Input		Not contained pull-down resistor $R = 1K\Omega$ (typ.)
OSC1 OSC2	Input Output		Oscillation terminals for OSD $R = 1K\Omega$ (typ.) $R_f = 1.5M\Omega$ (typ.) $R_O = 2K\Omega$ (typ.)
\overline{HD} \overline{VD}	Input		Synchronous signal input Hysteresis input $R = 1K\Omega$ (typ.)

(2) I/O port
The input/output circuit of the 47P834 is different to any I/O code of the 47C434/634/834. When this chip is used as evaluator with the I/O code, it is necessary to provide such as external resistors.

port \ I/O code	PB	PC	PF
K0	Pull-up resistor	Pull-down resistor	Pull-down resistor
R4, R50	—	—	Level shifter

Table 1-1. External Circuitry Corresponding to I/O Codes

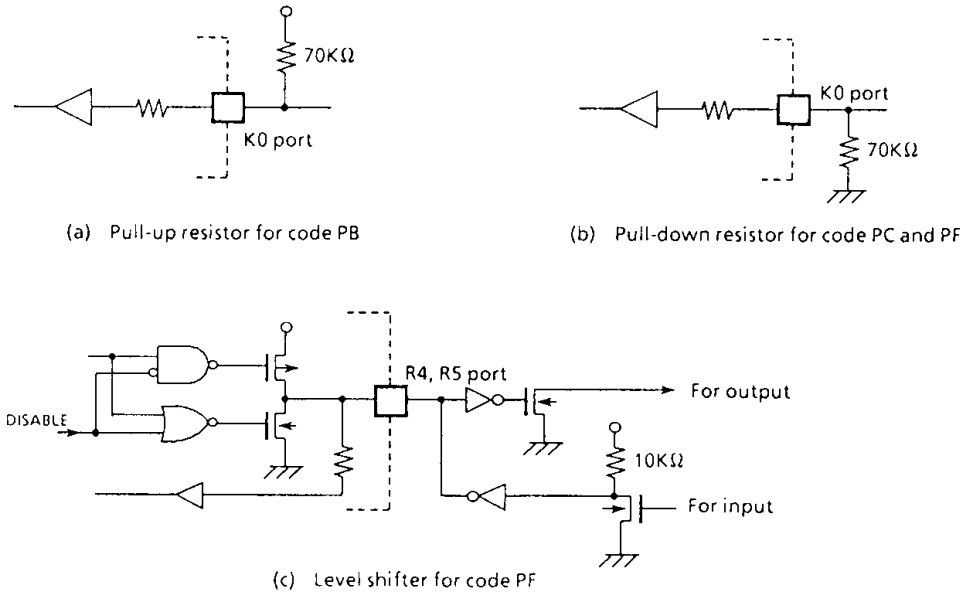
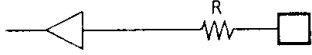
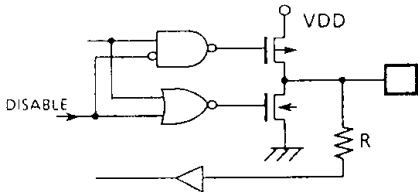
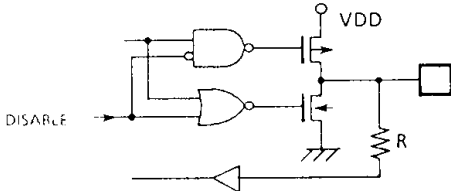
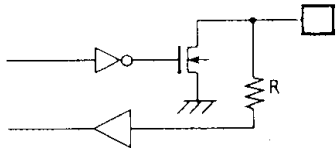
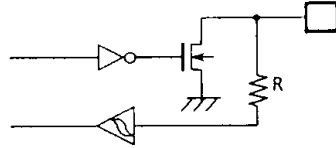
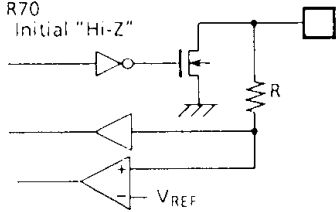
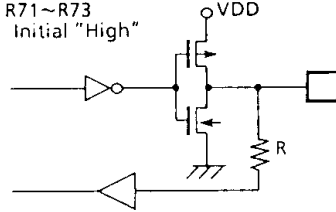
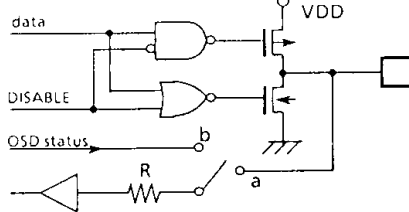
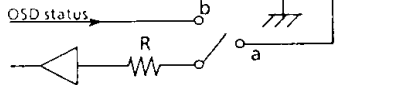


Figure 1-2. Example of External Circuitry

The input/output circuitry of the 47P834 I/O port is as follows.

PORT	I/O	INPUT/OUTPUT CIRCUITRY	REMARKS
K0	Input		Not contained Pull-up or pull-down resistor $R = 1K\Omega$ (typ.)
R4 R50	I/O		Tri-state Initial "Hi-Z" $R = 1K\Omega$ (typ.)
R51 R52 R53	I/O		Tri-state Initial "Hi-Z" $R = 1K\Omega$ (typ.)
R6 R8 R9	I/O	<div style="display: flex; justify-content: space-around;"> <div style="text-align: center;"> <p>R6</p>  </div> <div style="text-align: center;"> <p>R8, R9</p>  </div> </div>	Sink open drain Initial "Hi-Z" Hysteresis input (R8, R9) $R = 1K\Omega$ (typ.)
R7	I/O	<div style="display: flex; justify-content: space-around;"> <div style="text-align: center;"> <p>R70 Initial "Hi-Z"</p>  </div> <div style="text-align: center;"> <p>R71~R73 Initial "High"</p>  </div> </div>	Sink open drain and push-pull Comparator input (R70 pin) $R = 1K\Omega$ (typ.)
R (RA0) G (RA1)	I/O		Tri-state Initial "Hi-Z" $R = 1K\Omega$ (typ.)
B Y (BL)	Output		R, G : Side a B, Y : Side b

1.2 PROM mode

The PROM mode is set by setting the $\overline{\text{RESET}}$, $\overline{\text{HOLD}}$, R and G pins to the "L" level. The PROM mode can be used as a general-purpose PROM writer for program writing and verification. (A high-speed program mode is used set the ROM type the same as for the TMM 27128A.)

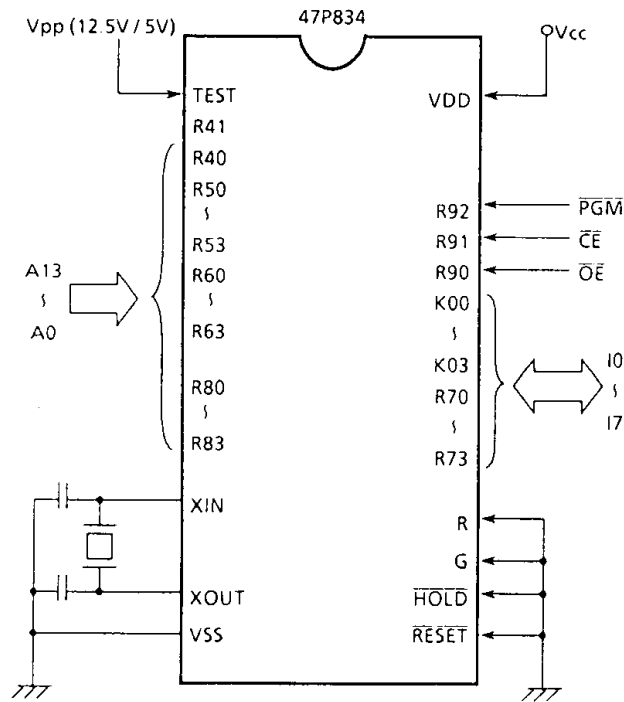


Figure 1-3. Setting for PROM mode

1.2.1 High speed programming mode

The device is set up in the high speed programming mode when the programming voltage (12.5V) is applied to the Vpp pin with Vcc = 6V and PGM = VIH4. The programming is achieved by applying a single TTL low level 1 msec, pulse the PGM input after addresses and data are stable. Then the programmed data is verified by using Program Verify mode. If the programmed data is not correct, another program pulse of 1 msec is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 15 times) After correctly programming the selected address, one additional program pulse with pulse width 4 times that needed for programming is applied. When programming has been completed, the data in all addresses should be verified with Vcc = Vpp = 5V.

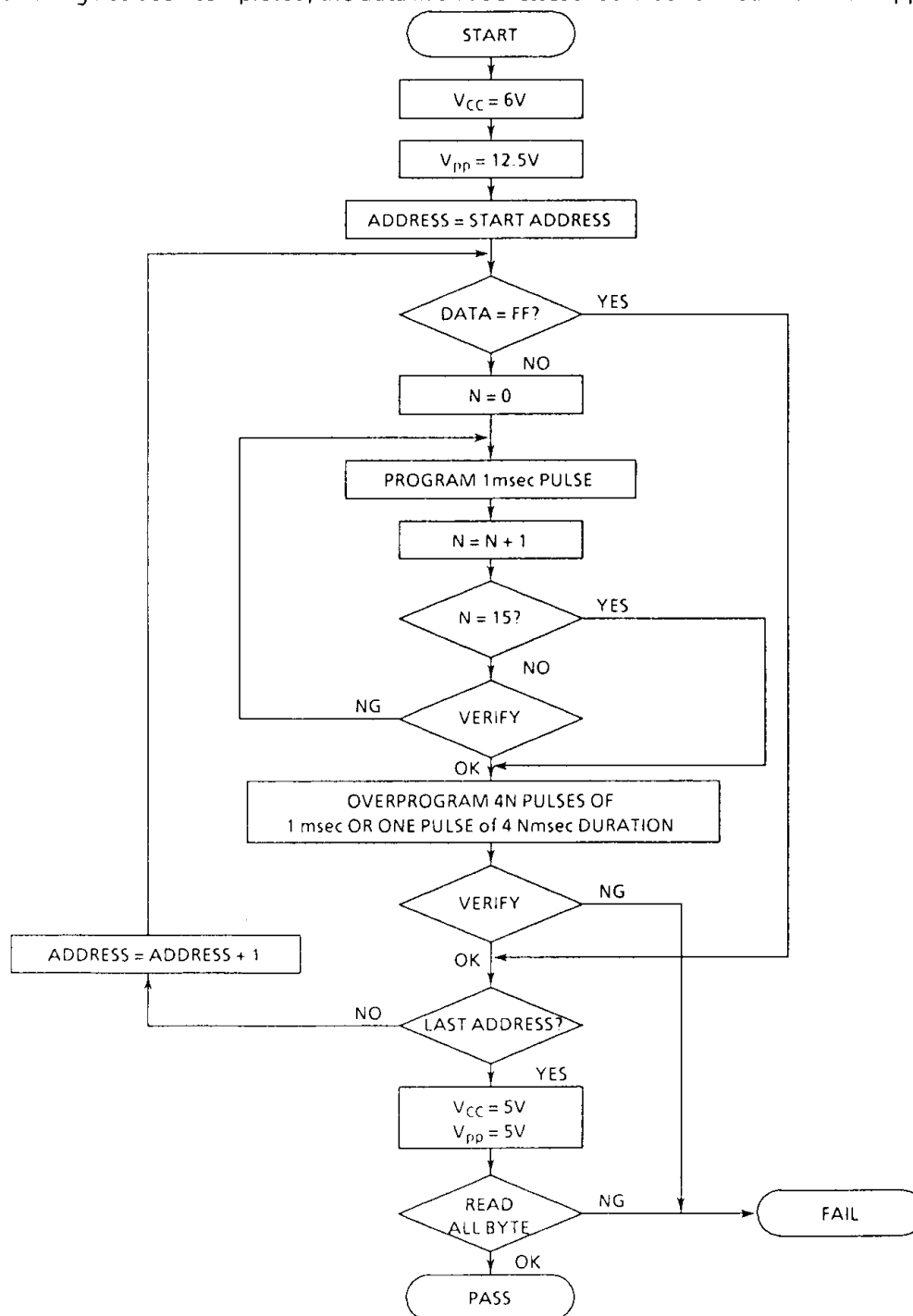


Figure1-4. FLOW CHART

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0V)

PARAMETER	SYMBOL	PINS	RATING	UNIT
Supply Voltage	V _{DD}		− 0.3 to 7	V
Input Voltage	V _{IN}		− 0.3 to V _{DD} + 0.3	V
Output Voltage	V _{OUT1}	Except sink open drain pin	− 0.3 to V _{DD} + 0.3	V
	V _{OUT2}	Sink open drain pin except R7 port	− 0.3 to 10	
Output Current (Per 1 pin)	I _{OUT1}	R6 port	30	mA
	I _{OUT2}	R7, R8, R9 port	3.2	
Output Current (Total)	Σ I _{OUT1}	R6 port	60	mA
Power Dissipation	PD		600	mW
Soldering Temperature (time)	T _{sld}		260 (10sec)	°C
Storage Temperature	T _{stg}		− 55 to 125	°C
Operating Temperature	T _{opr}		− 30 to 70	°C
Programming Voltage	V _{pp}	TEST / VPP pin	− 0.3 to 14.0	V

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V, T_{opr} = − 30 to 70 °C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Max.	UNIT
Supply Voltage	V _{DD}		in the Normal mode	4.5	6.0	V
			in the HOLD mode	2.0		
Input High Voltage	V _{IH1}	Except Hysteresis Input	V _{DD} ≥ 4.5V	V _{DD} × 0.7	V _{DD}	V
	V _{IH2}	Hysteresis Input		V _{DD} × 0.75		
	V _{IH3}		V _{DD} < 4.5V	V _{DD} × 0.9		
Input Low Voltage	V _{IL1}	Except Hysteresis Input	V _{DD} ≥ 4.5V	0	V _{DD} × 0.3	V
	V _{IL2}	Hysteresis Input			V _{DD} × 0.25	
	V _{IL3}		V _{DD} < 4.5V		V _{DD} × 0.1	
Clock Frequency	f _c			0.4	4.2	MHz
	f _{OSD}			–	6.0	

Note. Input Voltage V_{IH3}, V_{IL3} : in the HOLD mode.

D.C. CHARACTERISTICS (V_{SS} = 0V, T_{opr} = -30 to 70°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	V _{HS}	Hysteresis Input		—	0.7	—	V
Input Current	I _{IN1}	K0 port, TEST, RESET, HOLD	V _{DD} = 5.5V,	—	—	± 2	μA
	I _{IN2}	R port (open drain)	V _{IN} = 5.5V / 0V				
Input Low Current	I _{IL}	R port (push-pull)	V _{DD} = 5.5V, V _{IN} = 0.4V	—	—	- 2	mA
Input Resistance	R _{IN1}	K0 port with pull-up/pull-down		30	70	150	KΩ
	R _{IN2}	RESET		100	220	450	
Output Leakage Current	I _{LO}	Tri-state R6, R8, R9 port (open drain)	V _{DD} = 5.5V, V _{OUT} = 5.5V	—	—	± 2	μA
Output High Voltage	V _{OH1}	R port (push-pull)	V _{DD} = 4.5V, I _{OH} = - 200μA	2.4	—	—	V
	V _{OH2}	R port (tri-state), OSD output	V _{DD} = 4.5V, I _{OH} = - 0.7mA	4.1	—	—	
Output Low Voltage	V _{OL1}	R7, R8, R9 port	V _{DD} = 4.5V, I _{OL} = 1.6mA	—	—	0.4	V
	V _{OL2}	R port (tri-state), OSD output	V _{DD} = 4.5V, I _{OL} = 0.7mA				
Output Low Current	I _{OL}	R6 port	V _{DD} = 4.5V, V _{OL} = 1.0V	—	20	—	mA
Supply Current (in the Nomal mode)	I _{DD}		V _{DD} = 5.5V f _c = 4MHz	—	5	10	mA
Supply Current (in the HOLD mode)	I _{DDH}		V _{DD} = 5.5V	—	0.5	10	μA

Note 1. Typ. values show those at T_{opr} = 25°C, V_{DD} = 5V.

Note 2. Input Current I_{IN1} : The current through resistor is not included, when the pull-up/pull-down resistor is contained.

Note 3. Supply Current : V_{IN} = 5.3V/0.2V

The K0 port is open when the pull-up / pull-down resistor is contained.
The voltage applied to the R port is within the valid range V_{IL} or V_{IH}.

A / D CONVERSION CHARACTERISTICS

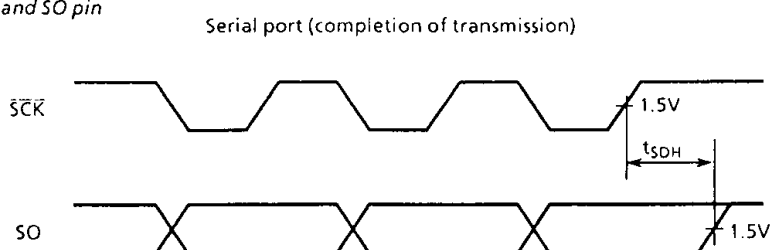
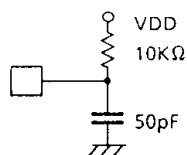
PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Analog Input Voltage	V _{AIN}	CIN		V _{SS}	—	V _{DD}	V
A/D Conversion Error	—			—	—	± 1/2	LSB

A.C. CHARACTERISTICS ($V_{SS} = 0V$, $V_{DD} = 4.5$ to $6.0V$, $T_{opr} = -30$ to $70^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT
Instruction Cycle Time	t_{cy}		1.9	—	20	μs
High level Clock Pulse Width	t_{WCH}	For external clock operation	80	—	—	ns
Low level Clock Pulse Width	t_{WCL}					
Shift Data Hold Time	t_{SDH}		$0.5t_{cy} - 300$	—	—	ns

Note: Shift data Hold Time

External circuit for $\overline{SC\bar{K}}$ pin and SO pin

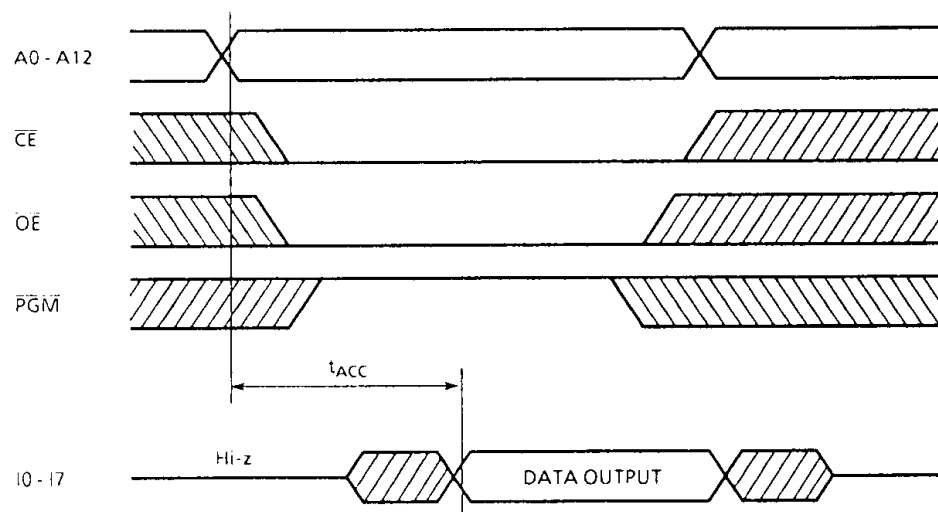

RECOMMENDED OSCILLATING CONDITIONS ($V_{SS} = 0V$, $V_{DD} = 4.5$ to $6.0V$, $T_{opr} = -30$ to $70^{\circ}C$)

Recommended oscillating conditions of the 47P834 are equal to the 47C834's.

DC/AC CHARACTERISTICS ($V_{SS} = 0V$)

(1) Read Operation

PARAMETER	SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT
Output Level High Voltage	V_{IH4}		$V_{CC} \times 0.7$	—	V_{CC}	V
Output Level Low Voltage	V_{IL4}		0	—	$V_{CC} \times 0.3$	V
Supply Voltage	V_{CC}		4.75	—	6.0	V
Programming Voltage	V_{PP}					
Address Access Time	t_{ACC}	$V_{CC} = 5.0 \pm 0.25V$	0	—	350	ns



(2) High Speed Programming Operation

PARAMETER	SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT
Input High Voltage	V_{IH4}		$V_{CC} \times 0.7$	—	V_{CC}	V
Input Low Voltage	V_{IL4}		0	—	$V_{CC} \times 0.3$	V
Supply Voltage	V_{CC}		4.75	—	6.0	V
V_{PP} Power Supply Voltage	V_{PP}		12.25	12.5	12.75	V
Programming Pulse Width	t_{PW}	$V_{CC} = 6.0 \pm 0.25V$	0.95	1.0	1.05	ms

